Past, Present, and Future Challenges for the IC Industry

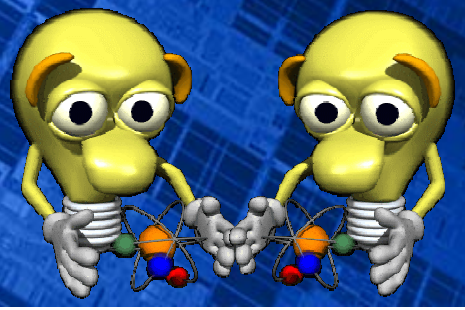
Paolo Gargini

Chairman ITRS

Sr. Member, IEEE

Director of Technology Strategy

Intel Fellow



The Issue of Power Consumption

Most of the Power was Consumed in Generating the Electrons!

Shockley Patent Notebook
(1945)

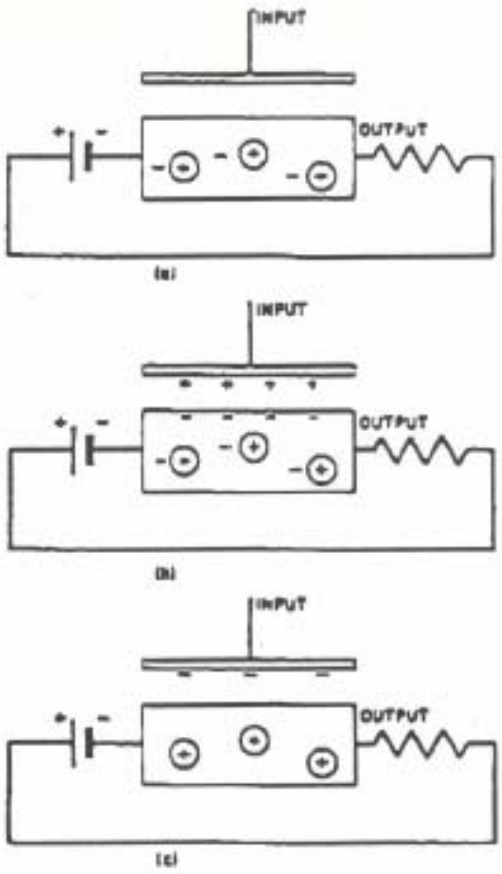
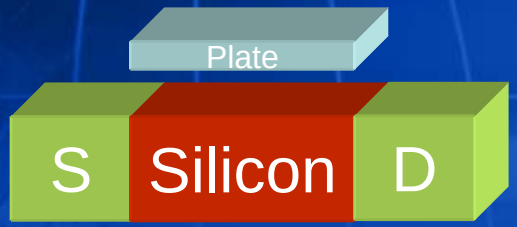


Fig. 6. The theory of a field-effect transistor using a thin layer of semiconductor: (a) The structure of the transistor with no control voltage applied. (b) The situation prevailing when a positive charge is placed on a control plate to increase the conductance of the semiconductor. (c) The situation when a negative charge is put on the capacitor plate to reduce the conductance of the semiconductor.

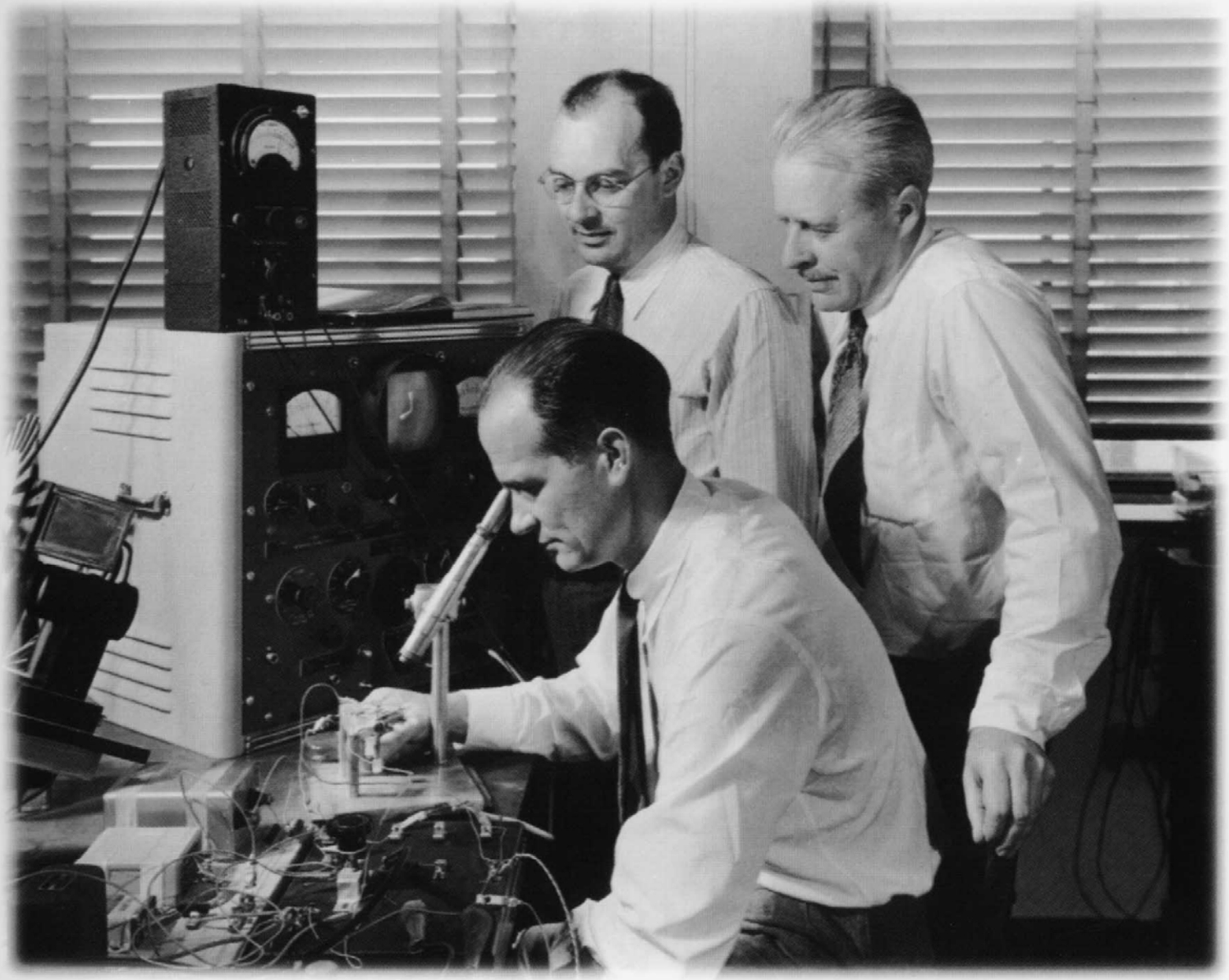
Early Failures of the MOS Device



- **1940-1945**. Scientists were unable to observe any conductivity modulation resulting from field effect on semiconductor surfaces
- **1946**. J. Bardeen formulated the surface states theory to explain the failure of the field-effect demonstrations

The Bipolar Transistor Only 60 years ago!

- 1947. J. Bardeen and W. Brattain invented and demonstrated the point-contact transistor
- 1948. W.B. Shockley invented the junction transistor.



William Shockley (seated), John Bardeen (standing left), and Walter Brattain in 1948.

Creative-Failure Methodology

"…failures of attempts to make field-effect transistors became <creative failures> by creating the program that discovered the point-contact transistor"

1963. W. B. Shockley

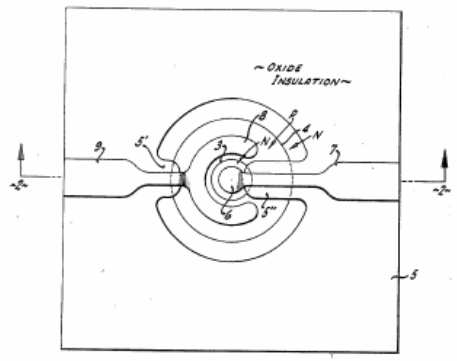
The First Planar Integrated Circuit 1961

April 25, 1961 R. N. NOYCE 2,981,877

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959 3 Sheets-Sheet 1

FIG-1



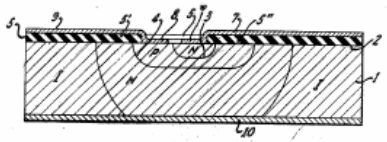
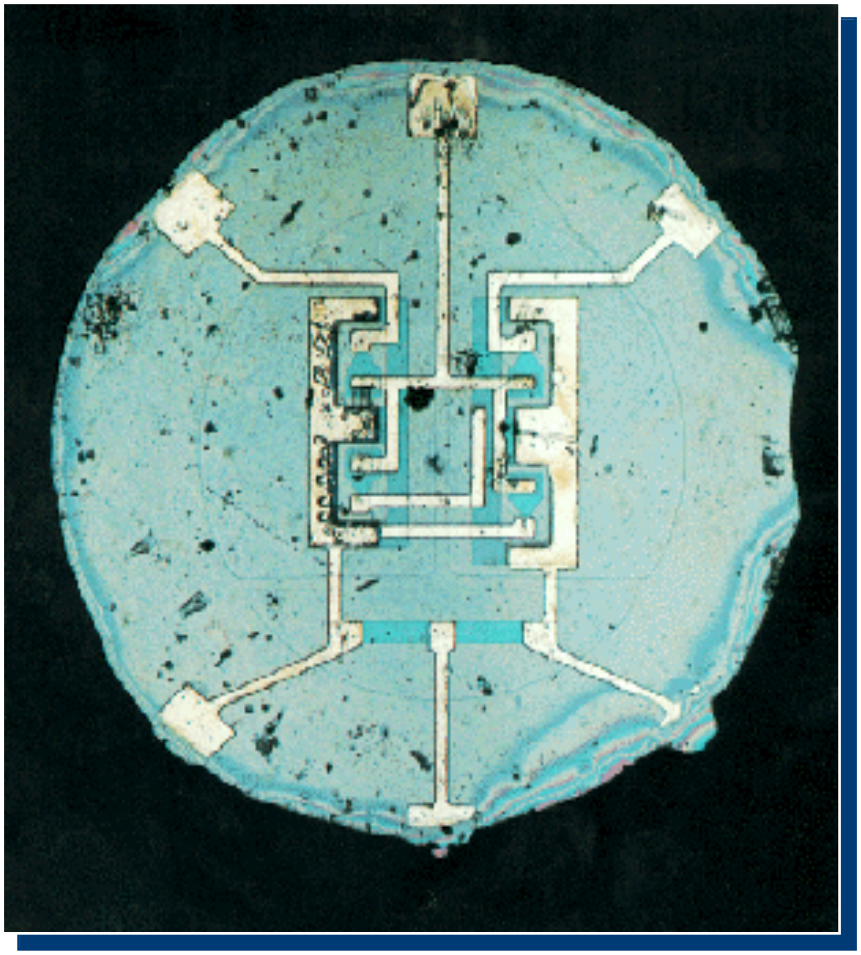
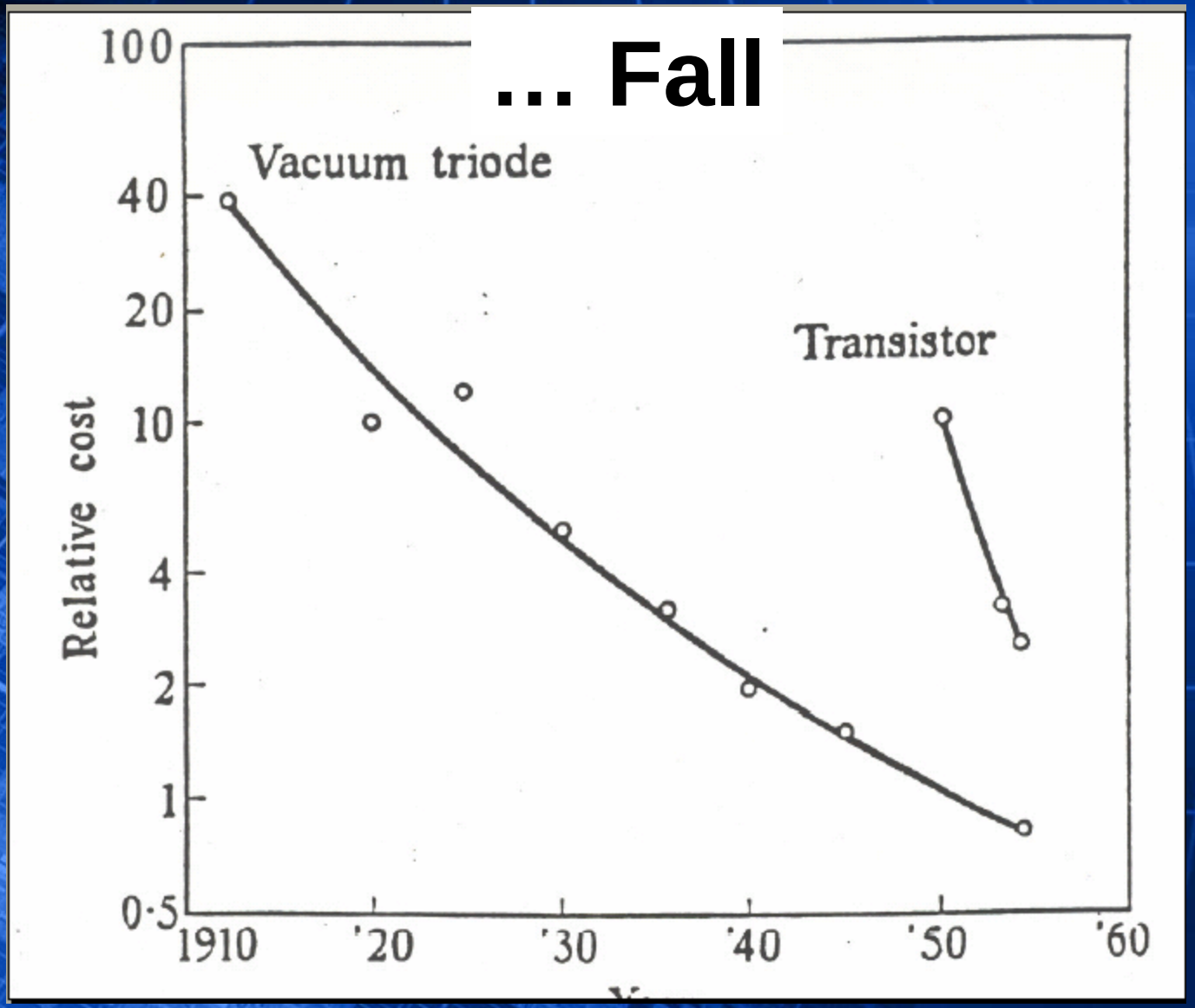


FIG-2

INVENTOR.
ROBERT N. NOYCE
BY Lappin & Kalb
ATTORNEYS



… Fall


Vacuum triode
Transistor
Relative cost
100
40
20
10
4
2
1
0·5
1910
'20
'30
'40
'50
'60
YEAR

Solving the Surface States Riddle 1964-1965

Solid-State Electronics Pergamon Press 1965. Vol. 8, pp. 145–163. Printed in Great Britain

INVESTIGATION OF THERMALLY OXIDISED SILICON SURFACES USING METAL–OXIDE–SEMICONDUCTOR STRUCTURES*

A. S. GROVE, B. E. DEAL, E. H. SNOW and C. T. SAH
Fairchild Semiconductor Division of Fairchild Camera and Instrument Corporation, Palo Alto, California

(*Received* 28 *May* 1964; *in revised form* 24 *July* 1964)

JOURNAL OF APPLIED PHYSICS VOLUME 36, NUMBER 12 DECEMBER 1965

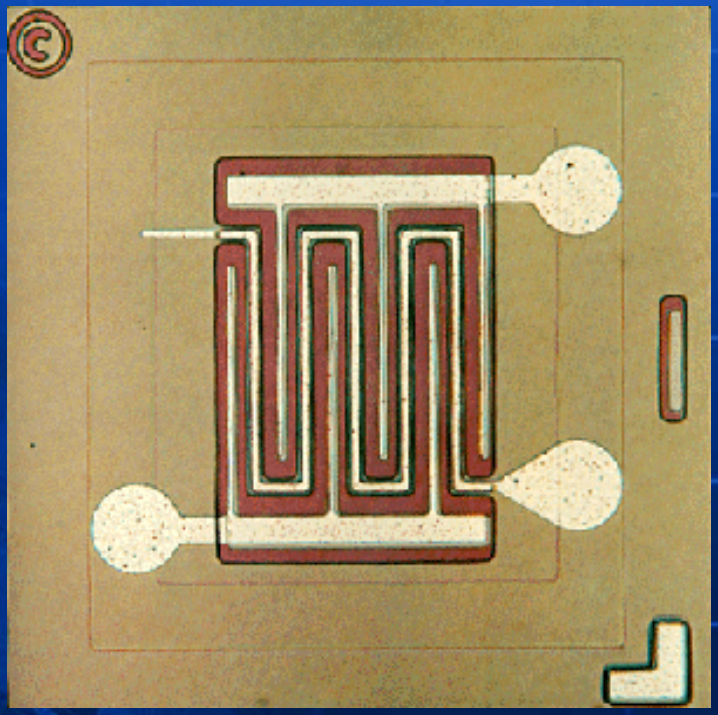
General Relationship for the Thermal Oxidation of Silicon

B. E. DEAL AND A. S. GROVE
Fairchild Semiconductor, A Division of Fairchild Camera and Instrument Corporation, Palo Alto, California

(Received 10 May 1965; in final form 9 September 1965)

1966: The First NMOS

- The first N-channel (depletion mode) MOS device.



FAIRCHILD SEMICONDUCTOR®

1967: Minimizing Surface States

J. Electrochem. Soc.: SOLID STATE SCIENCE *March 1967*

Characteristics of the Surface-State Charge (Q_{ss}) of Thermally Oxidized Silicon

B. E. Deal, M. Sklar, A. S. Grove, and E. H. Snow

Research and Development Laboratories, Fairchild Semiconductor, Palo Alto, California

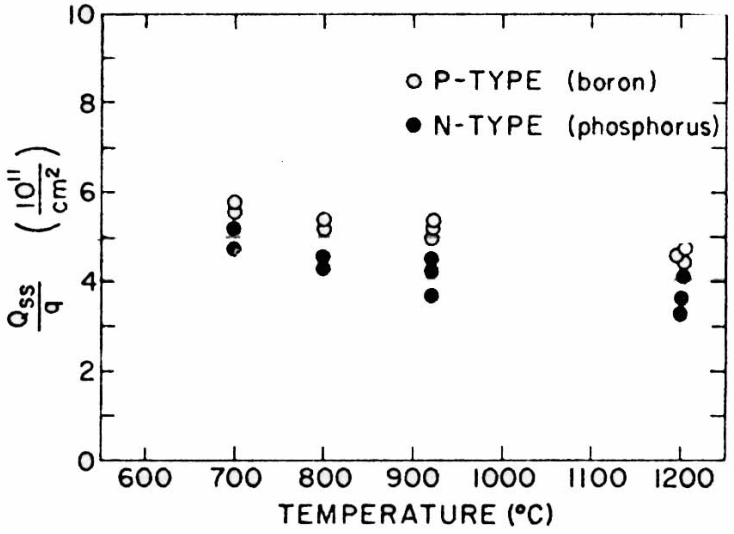


Fig. 4. Effect of oxidation temperature on the surface-state charge density Q_{ss}—wet oxygen (95°C H_2O) [$x_o = 0.20\mu$; N_A, $N_D = 1.4 \times 10^{16}$ cm^{-3}; (111) orientation].

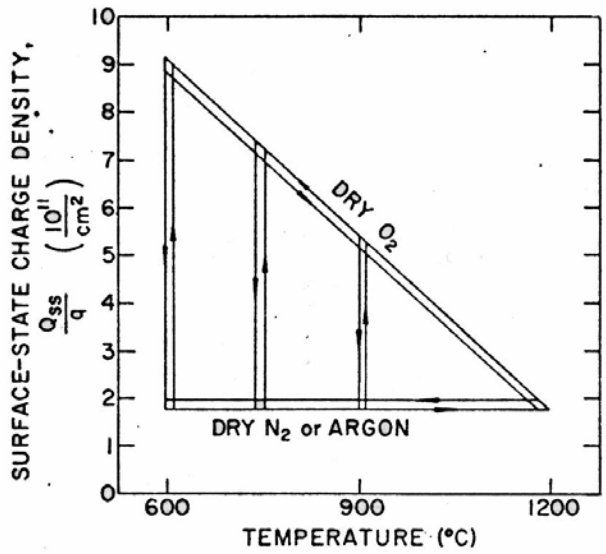


Fig. 5. Illustration of the reversibility of heat treatment effects on the surface-state charge density Q_{ss}.

The Silicon Gate Takes Off!

IEEE Spectrum October, 1969 28

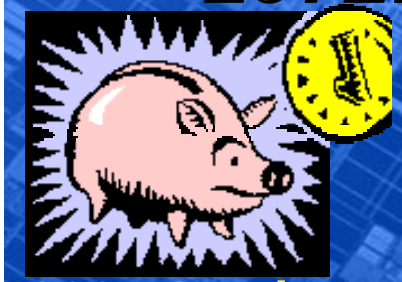
Silicon-gate technology

Low-cost, large-scale integrated electronics based on metal-oxide-semiconductor design benefits from the application of silicon-gate technology

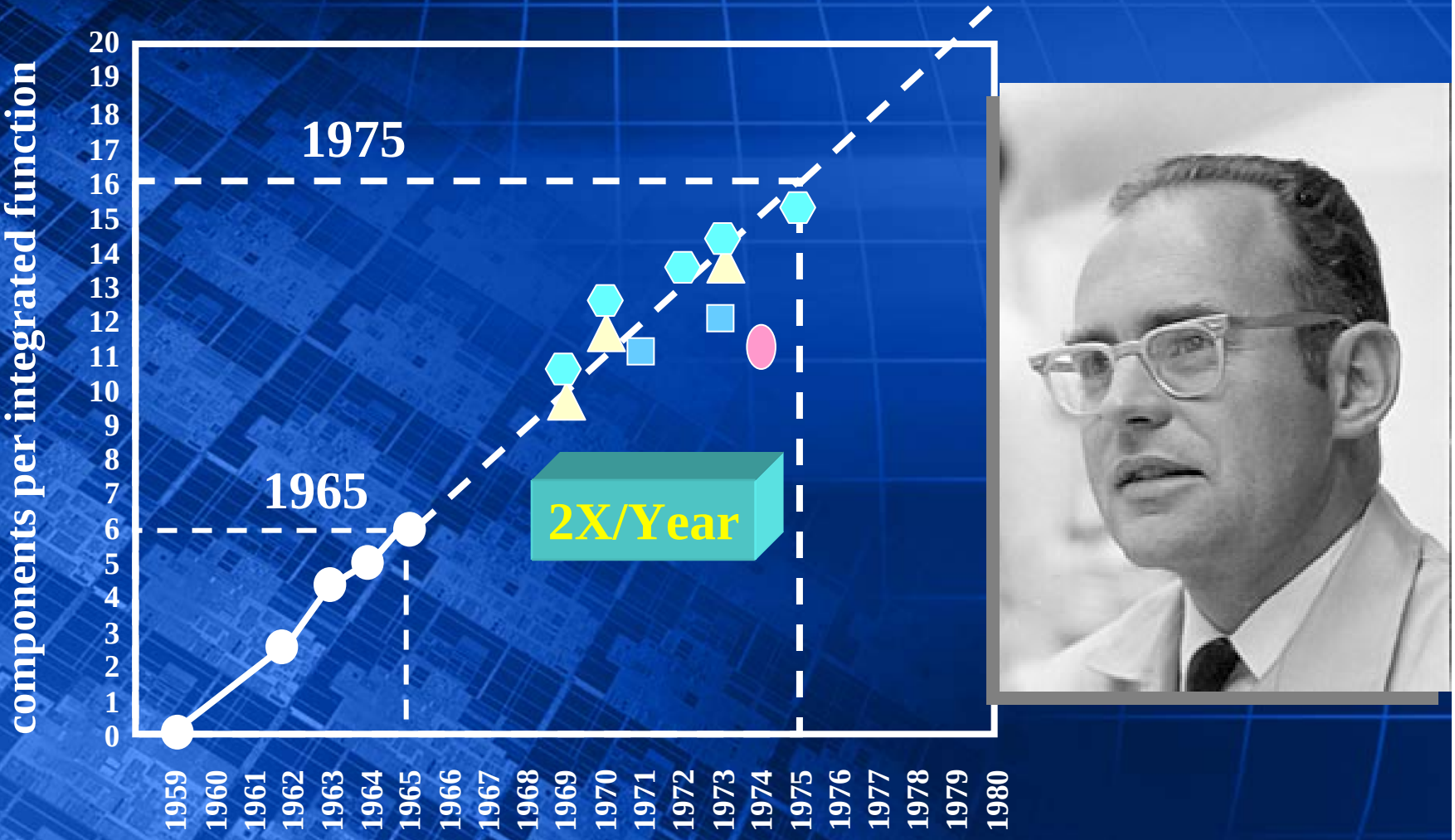
L. L. Vadasz, A. S. Grove, T. A. Rowe, G. E. Moore Intel Corporation

Commercialization of MOS

- 1969. 1101, 6T, 256 SRAM produced
- 1970. 1103, 3T, 1Kbit DRAM produced
- 1971. 2101/2, 6T, 1Kbit SRAM produced
- 1971. 1702, 2Kbit EPROM produced
- 1971. 4004 MPU produced
- 1972. 2104,1T, 4Kbit DRAM produced



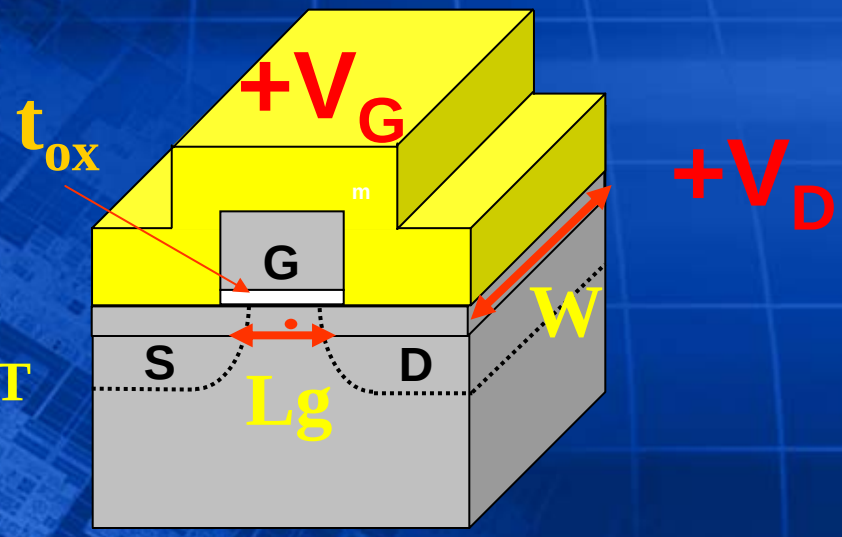
Second Update of Moore's Law



International Electron Device Meeting, December 1975

Transistor Components

$V_G = V_D = V_{DD} - V_T$

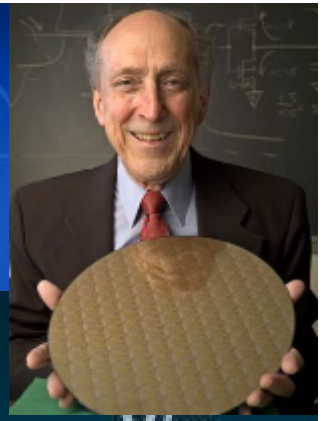


Vertical | Horizontal | Performance

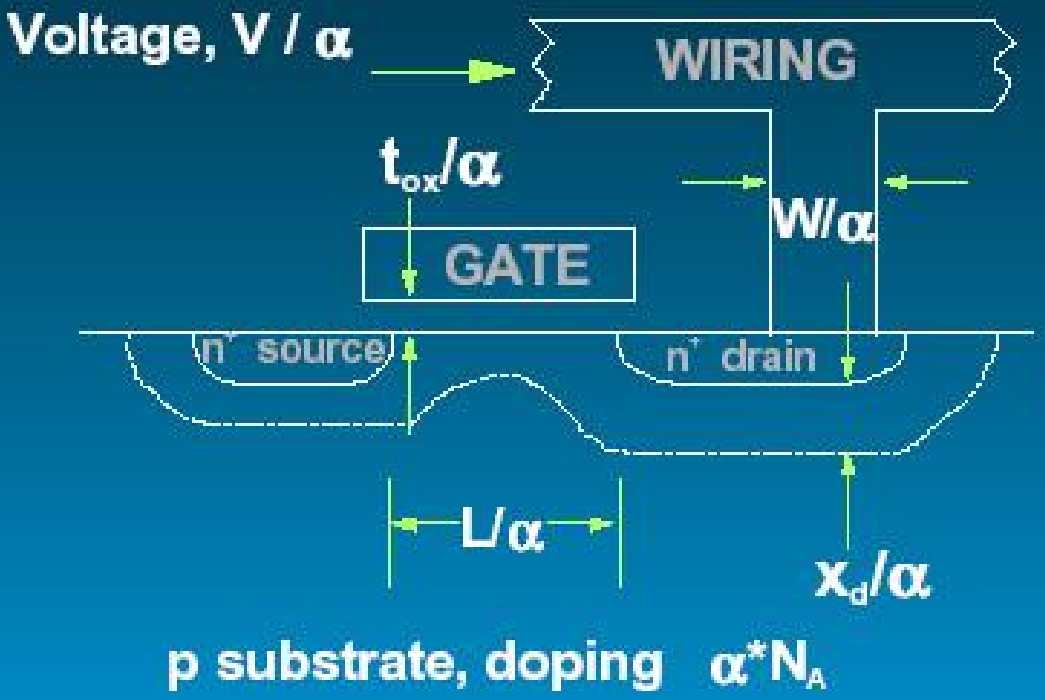
$$\frac{I_{DSat}}{W} \sim \frac{1}{2}\left[\frac{\varepsilon_o\,\varepsilon_s}{t_{ox}}\right]\left[\frac{\mu}{Lg}\right](V_{DD} - V_T)^2$$

Charge | Density | Power

MOS Transistor Scaling



Scaled Device



p substrate, doping $\alpha^* N_A$

SCALING:

Voltage:	V/α
Oxide:	t_{ox}/α
Wire width:	W/α
Gate width:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha * N_A$

RESULTS:

Higher Density:	$\sim\alpha^2$
Higher Speed:	$\sim\alpha$
Lower Power/ckt:	$\sim 1/\alpha^2$
Power Density:	~Constant

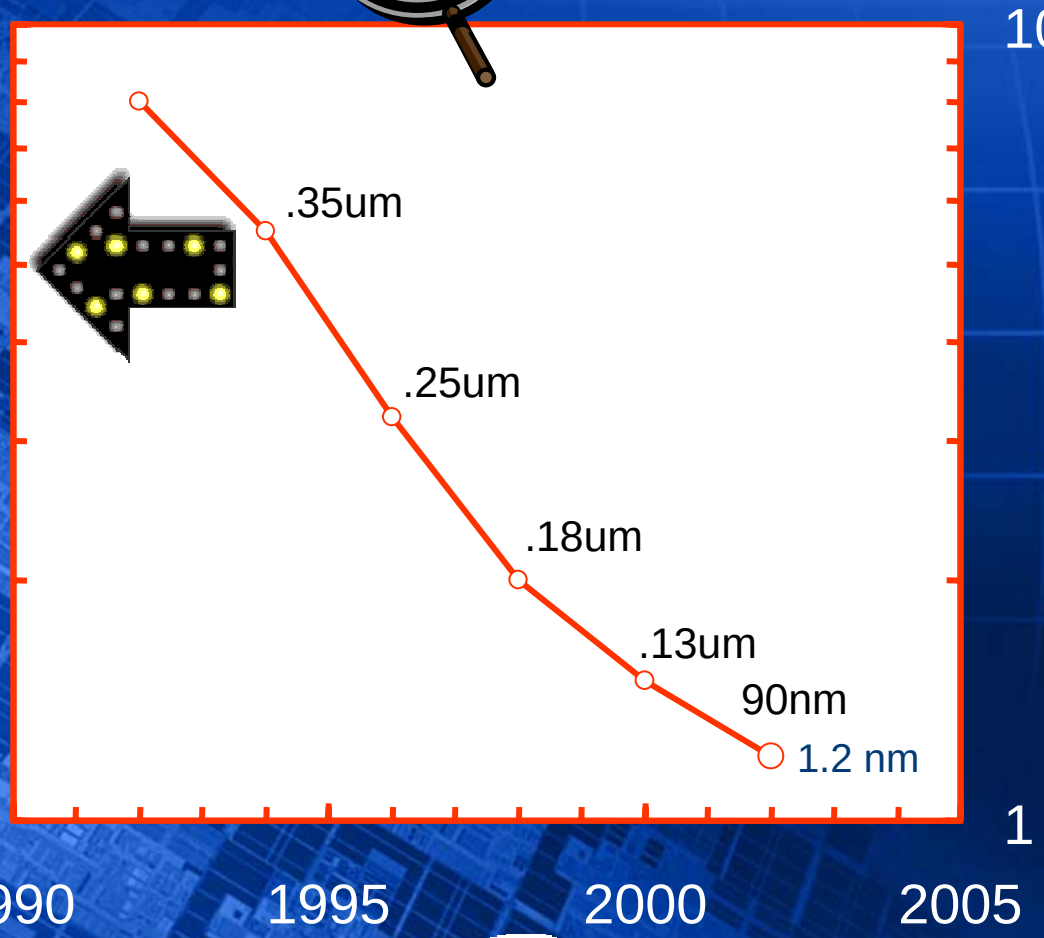
Scaling

Scaling

Scaling

Gate Oxide Scaling: Charge

$$\frac{I_{DSat}}{W} \sim \frac{1}{2} \cdot \frac{\varepsilon_o \varepsilon_s}{} \cdot \frac{\mu}{Lg} \cdot (V_{DD} - V_T)^2$$



1994 NTRS

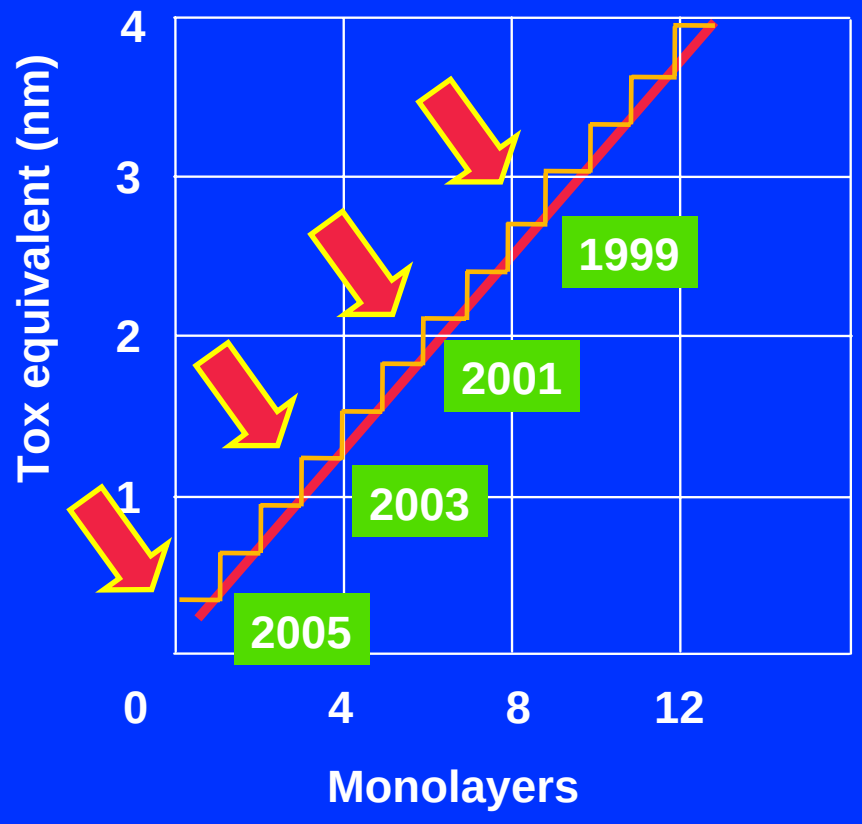
	1995 0.35 µm	*1998 0.25 µm*	*2001 0.18 µm*	*2004 0.13 µm*	*2007 0.10 µm*	*2010 0.07 µm*
Isolation	**LOCOS/ STI †/SOI**	**STI †/SOI**				
Gate oxide	**thermal**	**thermal/rapid thermal oxidation**				
Gate electrode		**n; n/p poly; poly/ silicide**				
Source/drain	**LDD*/MDD‡; S/D ext**	**same + raised S/D**				
Interconnect	**planar**					
Wires	**Al based**	**Al, Cu (thick)**				
Interlevel dielectric	**oxide**	**oxide; air; polyimide; low dielectric**				
Via studs	**W**	**W/Al/Cu**				

**LDD - lightly doped drain*
†STI - shallow trench isolation
‡MDD - medium doped drain

Table 6 Logic Technology Characteristics

From My Files

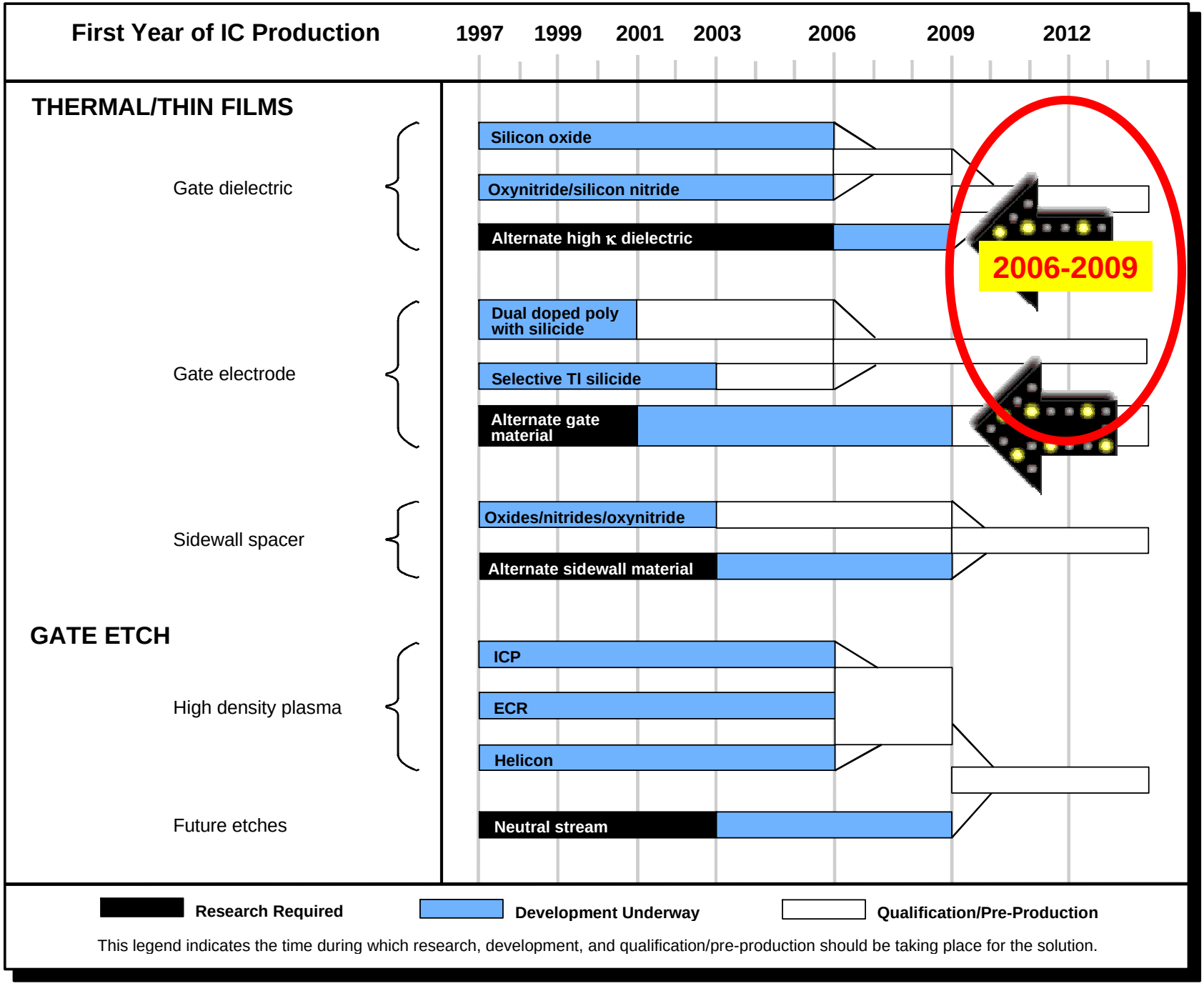
Gate Dielectric Scaling



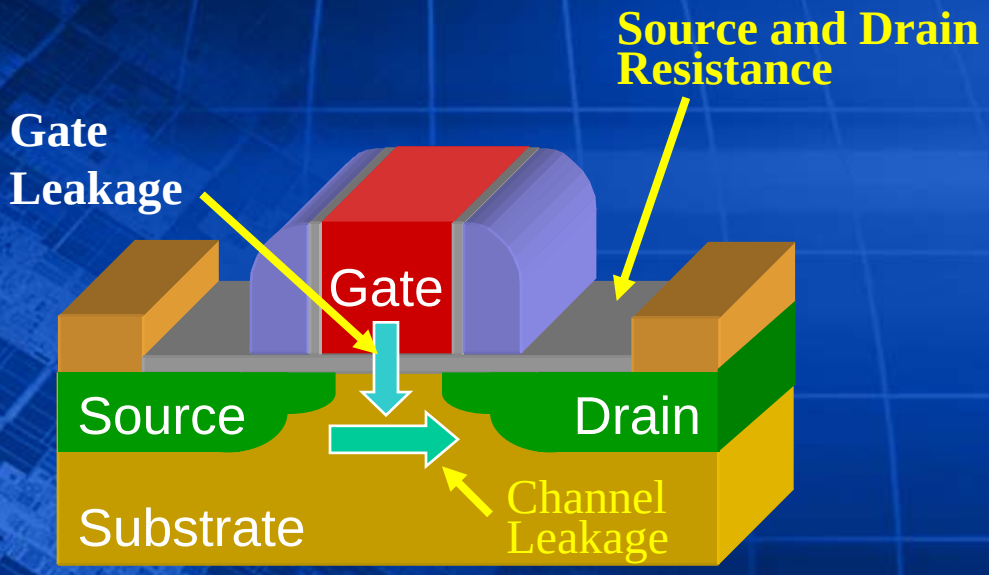
1997 NTRS

P.Gargini

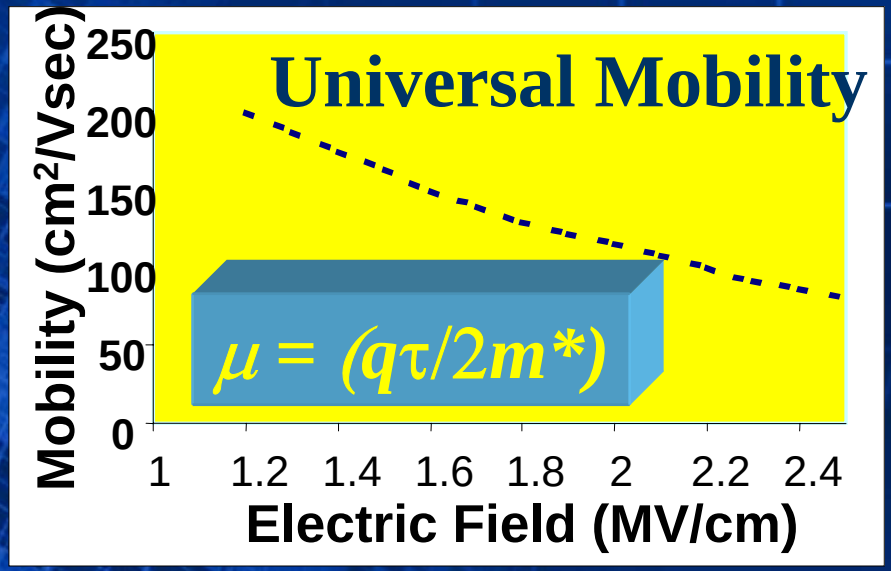
1997 NTRS


First Year of IC Production
1997
1999
2001
2003
2006
2009
2012
THERMAL/THIN FILMS
Gate dielectric
Silicon oxide
Oxynitride/silicon nitride
Alternate high κ dielectric
2006-2009
Gate electrode
Dual doped poly with silicide
Selective Tl silicide
Alternate gate material
Sidewall spacer
Oxides/nitrides/oxynitride
Alternate sidewall material
GATE ETCH
High density plasma
ICP
ECR
Helicon
Future etches
Neutral stream
Research Required
Development Underway
Qualification/Pre-Production
This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Geometrical Scaling Limitations



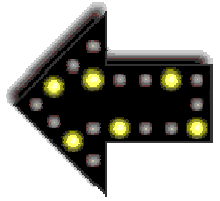
- S/D Leakage
- Gate Leakage
- S/D Resistance
- Decreased Mobility



1998 ITRS Update

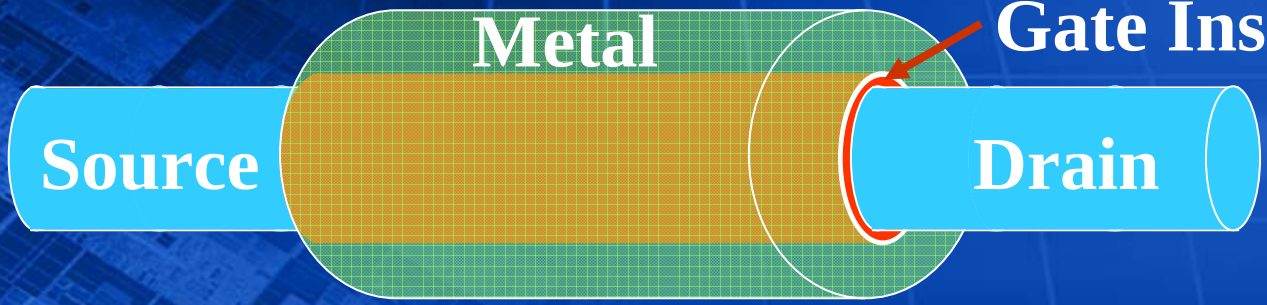
10th Anniversary of ITRS!

- Participation extended to: EECA, EIAJ, KSIA, TSIA at WSC on April 23,1998
- 1st Meeting held on July 10/11,1998 in San Francisco

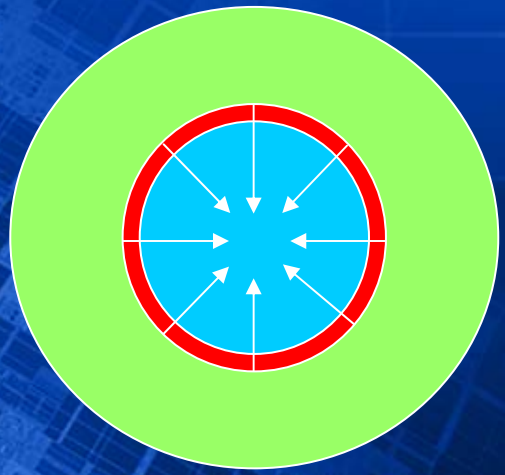


- 2nd meeting held on December 10/11,1998 at SFO
- 50% of tables in 1997 NTRS required some changes
- 1998 ITRS Update posted on web in April 1999

The Ideal MOS Transistor



Fully Surrounding Metal Electrode



Fully Enclosed, Depleted Semiconductor

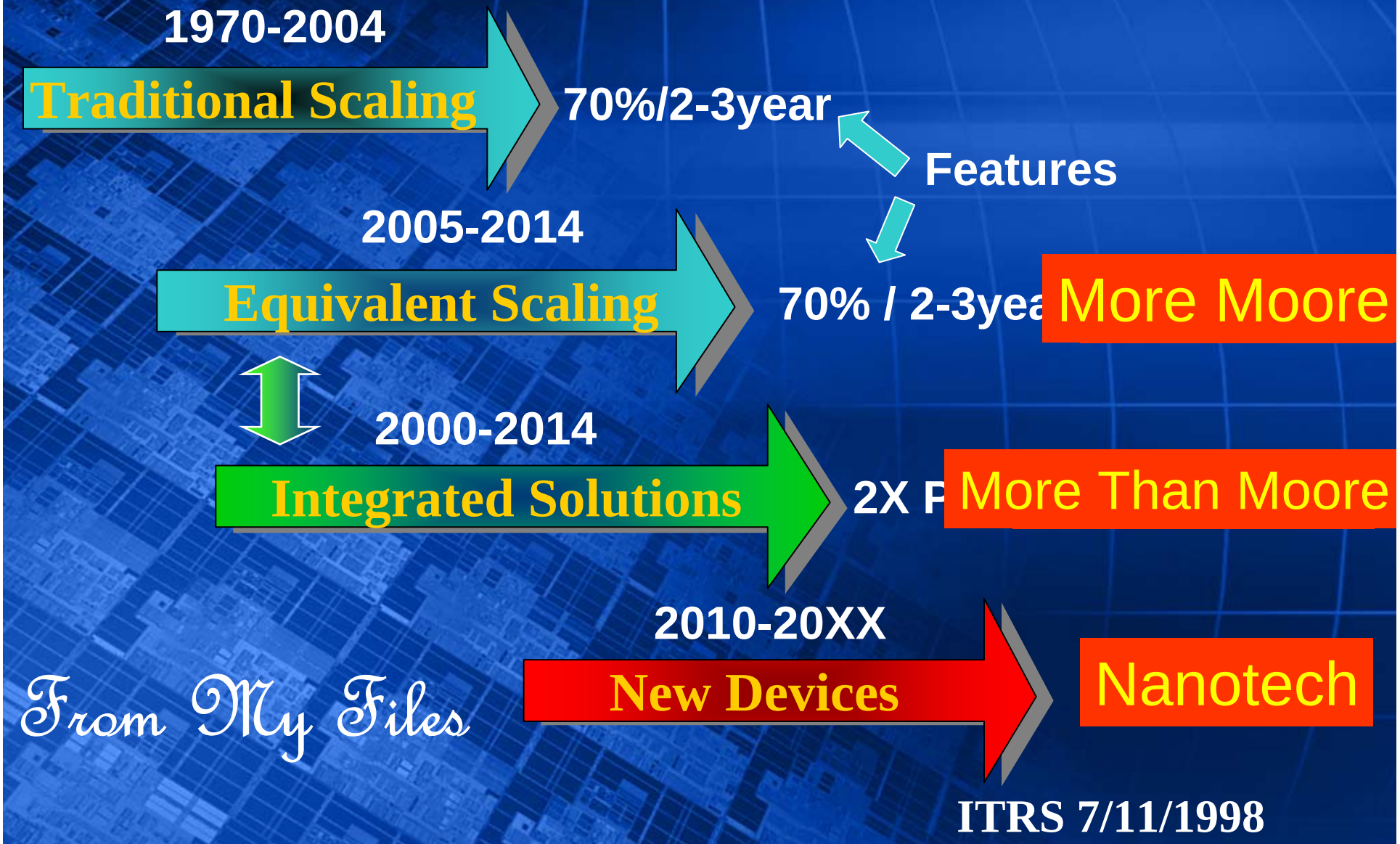
High-K Gate Insulator

Band Engineered Semiconductor

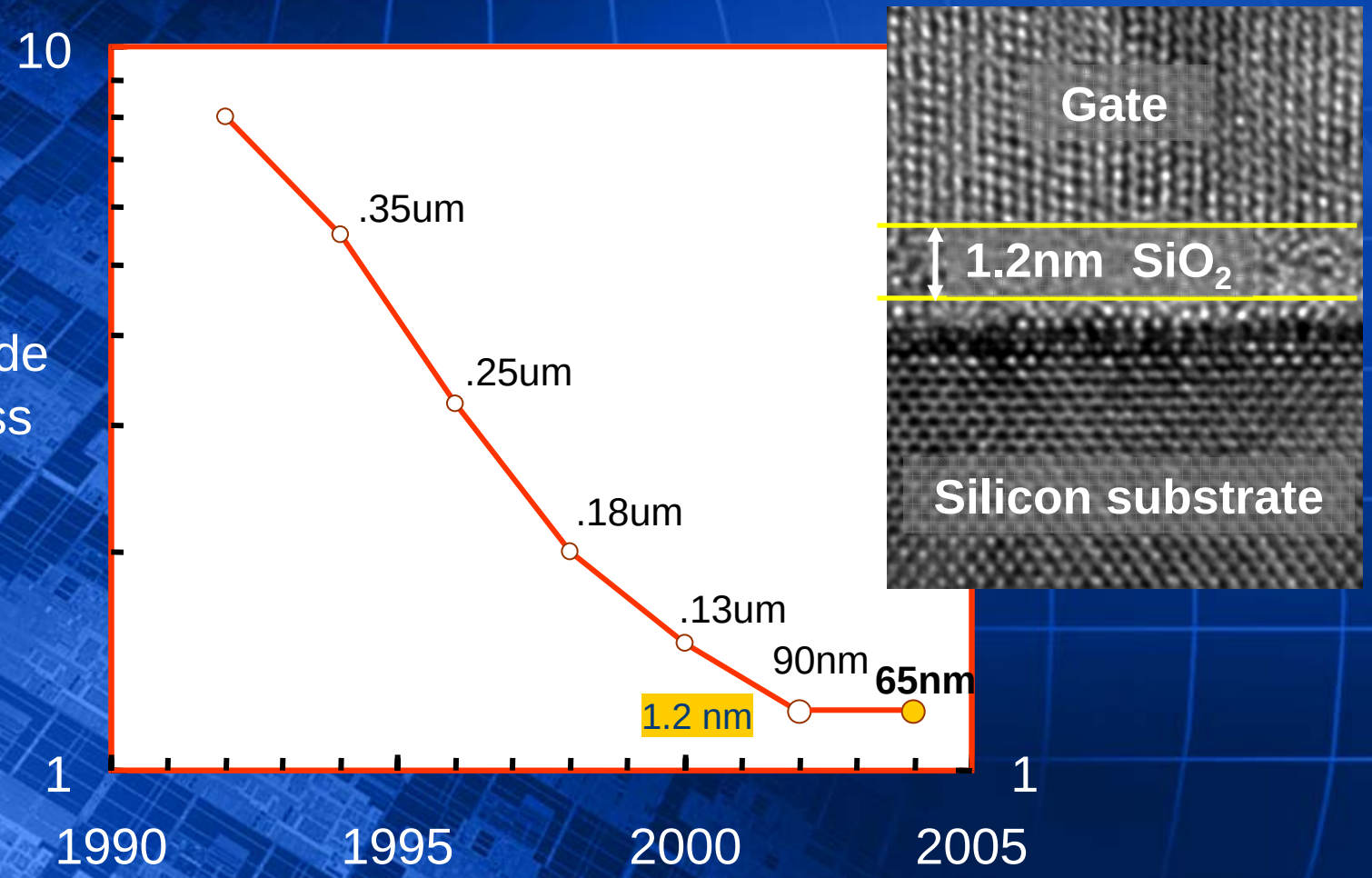
Low Resistance Source/Drain

From My Files

CMOS Future Directions



Gate Oxide Scaling



Gate oxide scaling is reaching its limits

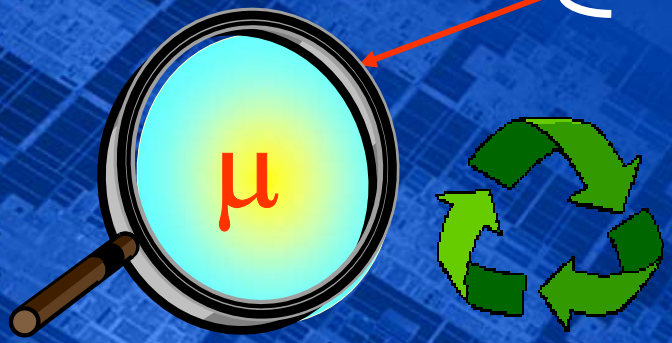
Source: Intel P.Gargini

New Transistor Trade-off

$$\frac{I_{DSat}}{W} \sim \frac{1}{2}\left[\frac{\varepsilon_o\,\varepsilon_s}{t_{ox}}\right]\left[\frac{\mu}{Lg}\right](V_{DD}-V_T)^2$$

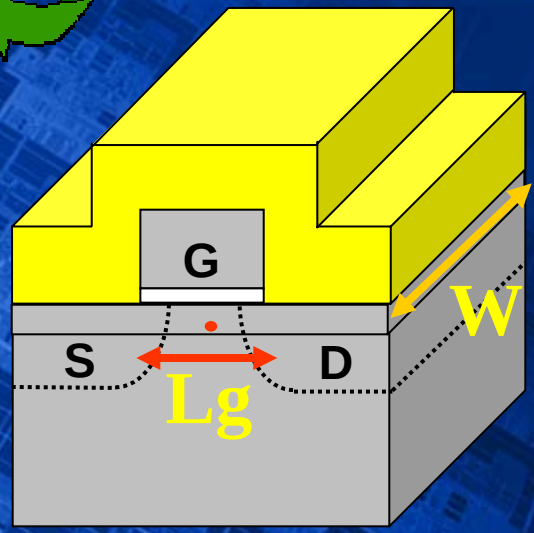
Reduce **Lg**

New Increase in Cox



Increase μ

New Increase in Performance

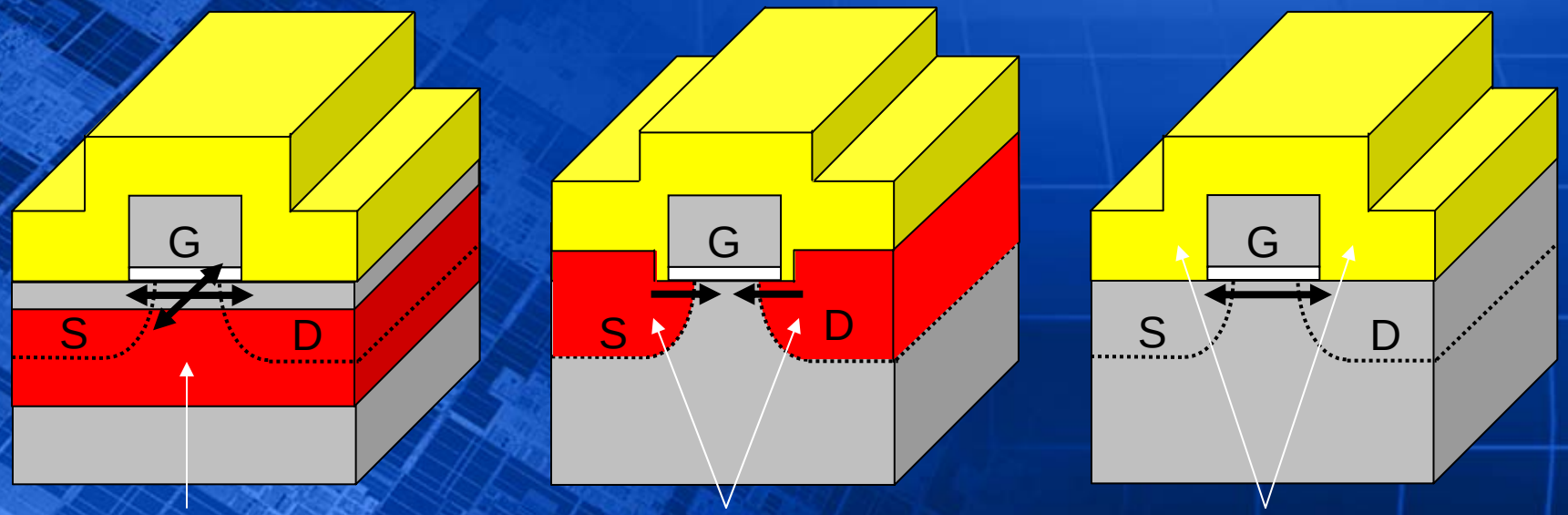


New Material

Transistor Strain Techniques

Traditional Approach

Intel's 90nm Technology



Graded SiGe Layer

Biaxial Tensile Strain

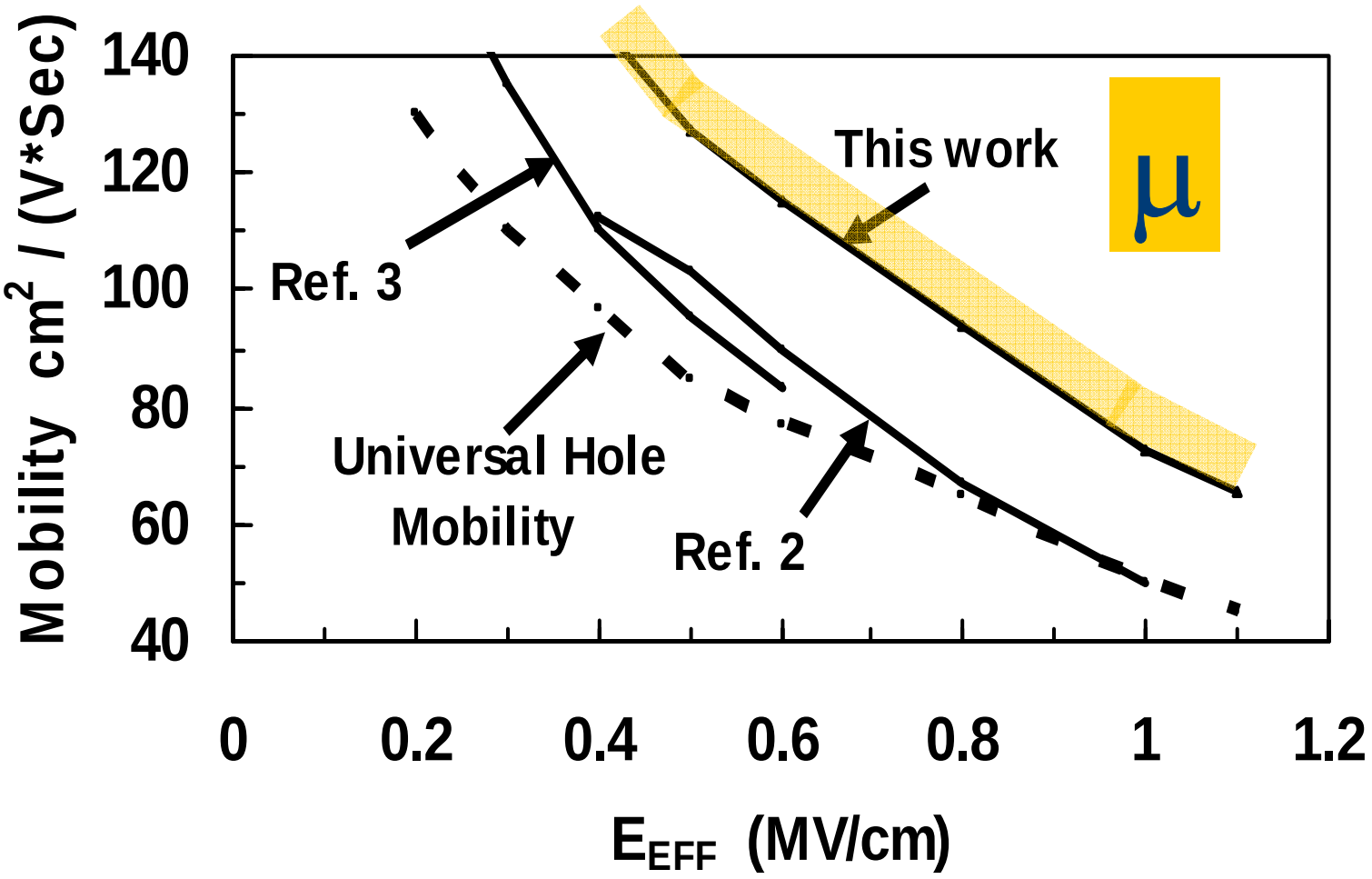
Selective SiGe S-D

Uniaxial Compressive Strain for PMOS

Tensile Si_3N_4 Cap

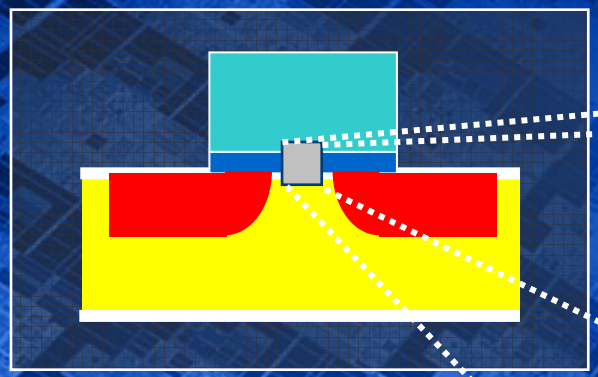
Uniaxial Tensile Strain for NMOS

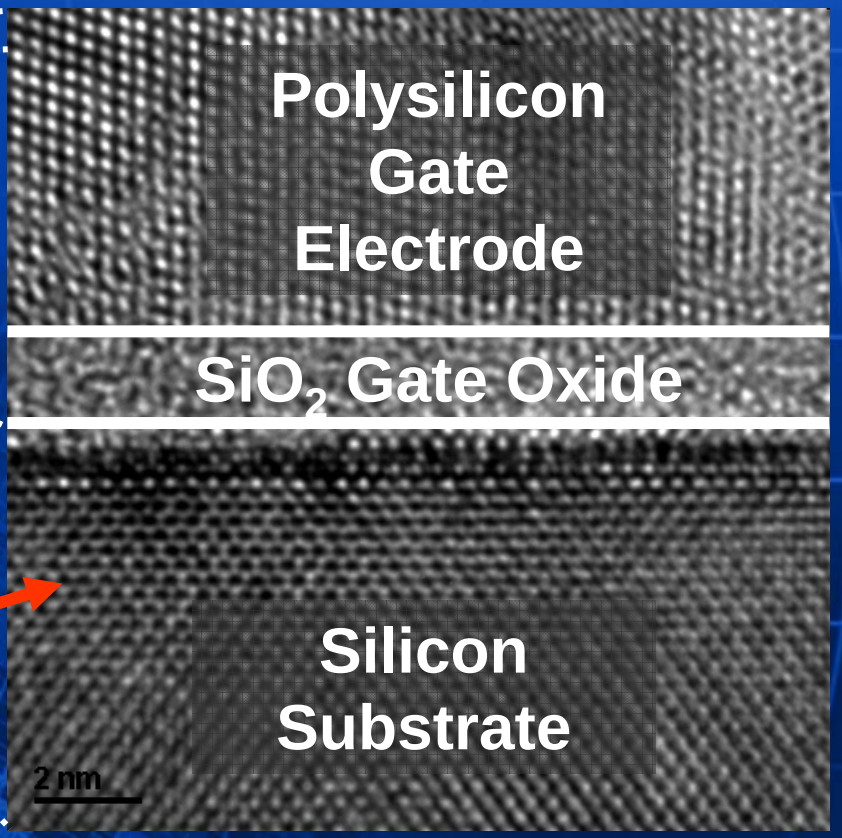
Hole Mobility as a Function of Vertical Effective Field



Source: T. Ghani, 2003 IEDM

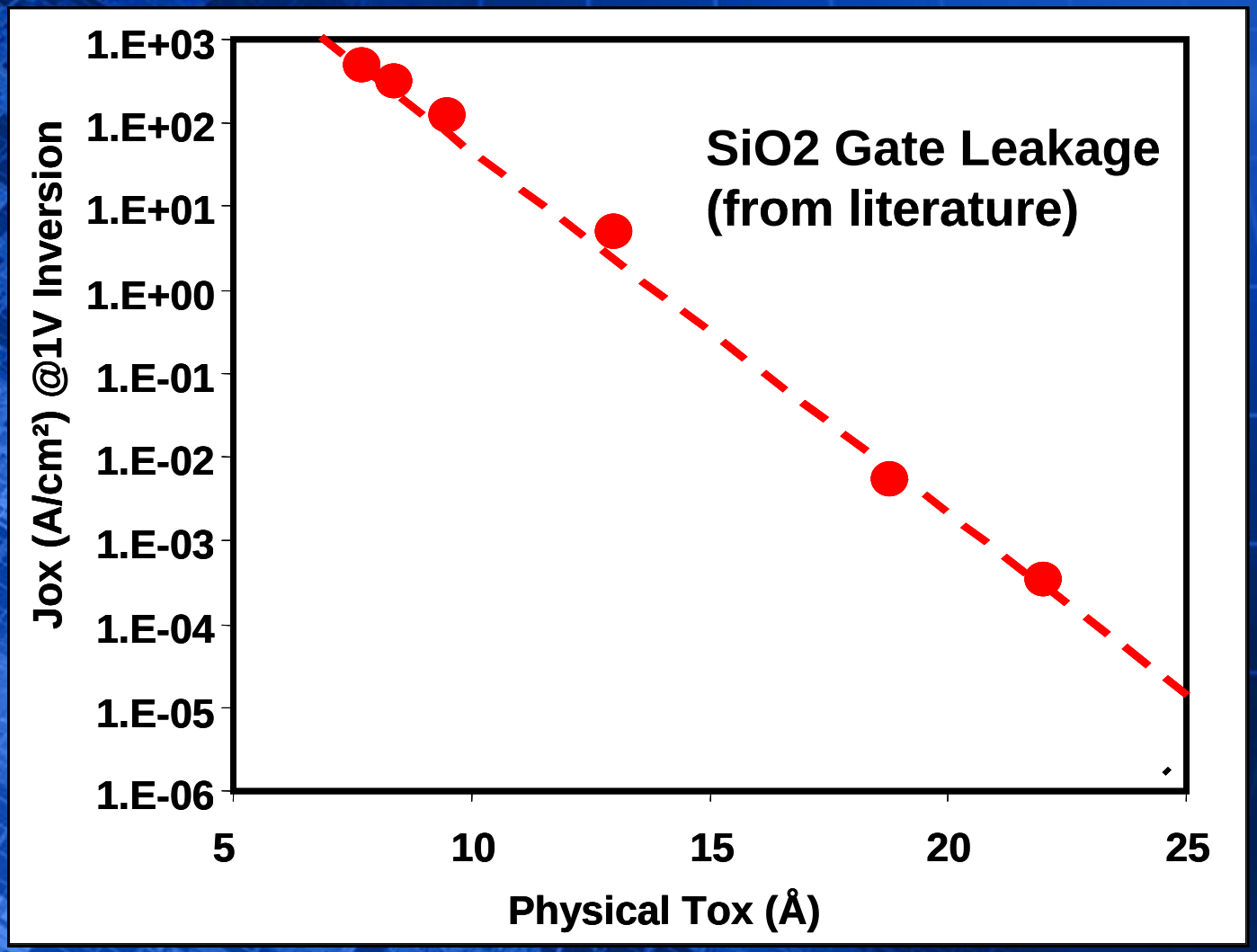
Gate Dielectric Today is Only a Few Molecular Layers Thick



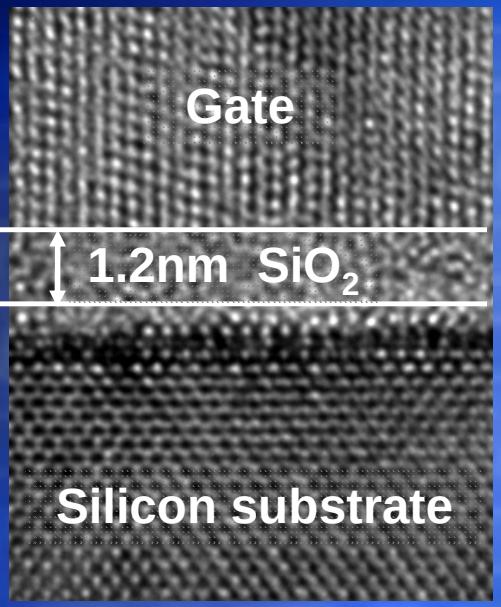


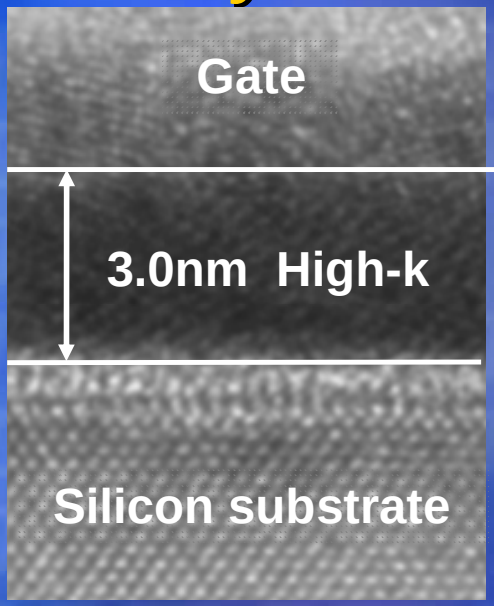
Individual Atoms

Thin Gates have More Leakage



High-k Dielectric reduces leakage substantially





Benefits compared to current process technologies

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Much faster transistors*
Gate dielectric leakage	> 100x reduction	*Far cooler*

Continuation of Moore's Law

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25μm	0.18μm	0.13μm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal

Introduction targeted at this time

Subject to change

Intel found a solution for High-k and metal gate

November 4th, 2003

45 nm Technology Benefits

- Compared to today's 65 nm technology, Intel's 45 nm technology will provide the following product benefits:

~2x improvement in transistor density, for either smaller chip size or increased transistor count

~30% reduction in transistor switching power

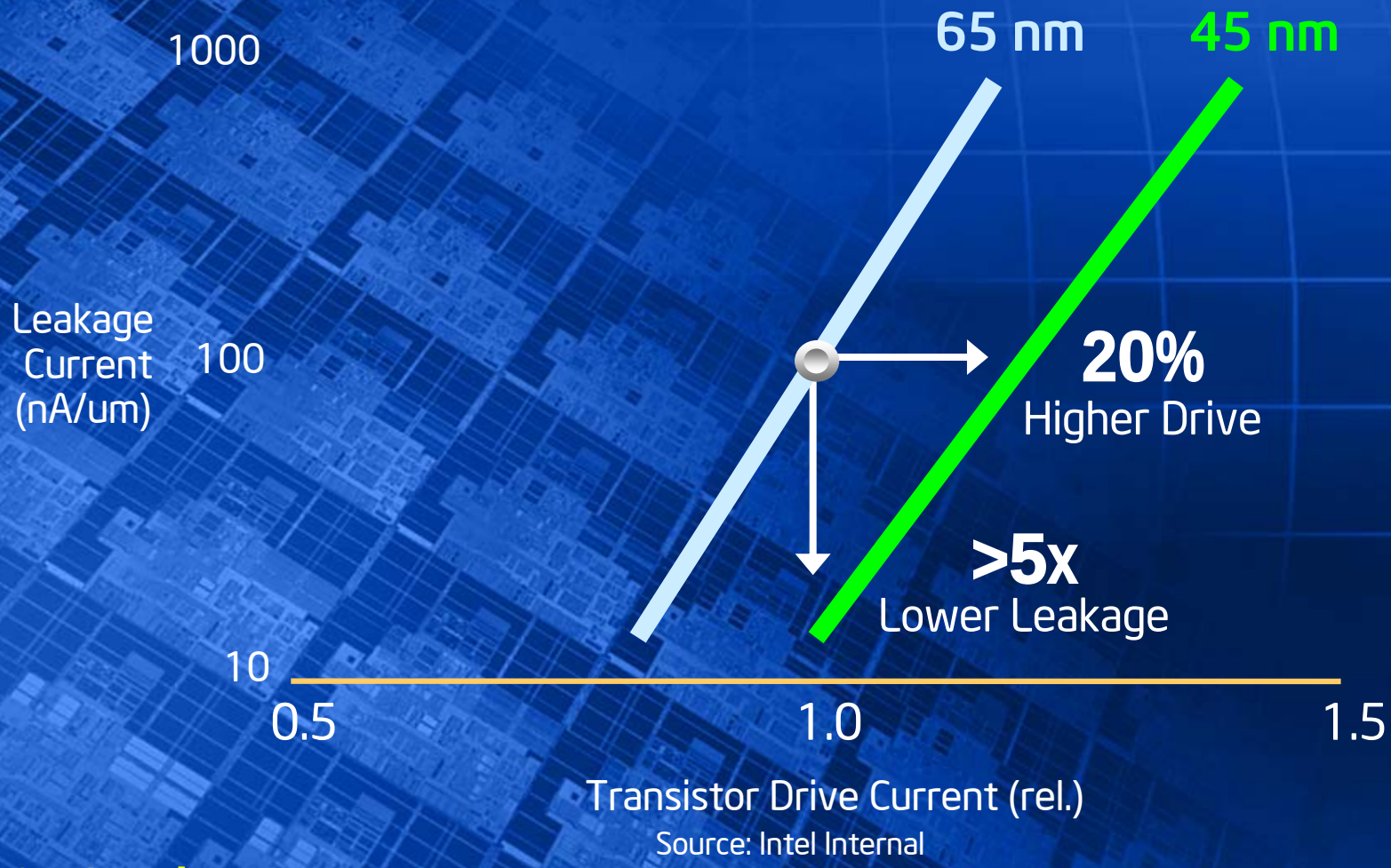
>20% improvement in transistor switching speed or
>5x reduction in source-drain leakage power

>10x reduction in gate oxide leakage power

- These performance and leakage improvements would not be possible without high-k + metal gate

45nm High-k Performance/Power Benefits

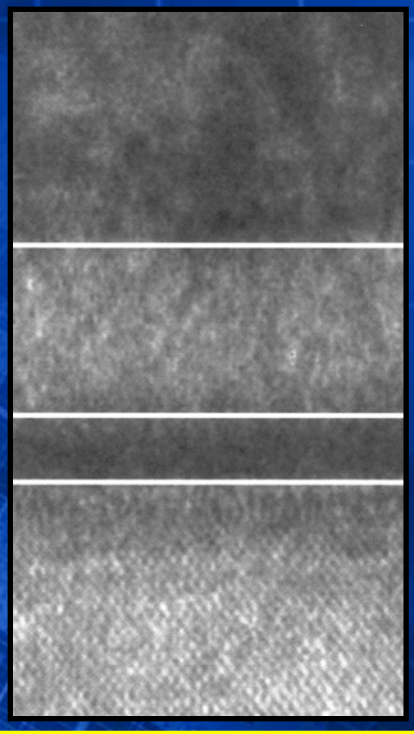
Transistor Performance vs. Leakage



Source: Intel Internal

High-k + Metal Gate Transistors

- ✓ Integrated 45 nm CMOS process
- ✓ High performance
- ✓ Low leakage
- ✓ Meets reliability requirements
- ✓ Manufacturable in high volume



Low Resistance Layer

Work Function Metal
Different for NMOS and PMOS

High-k Dielectric
Hafnium based

Silicon Substrate

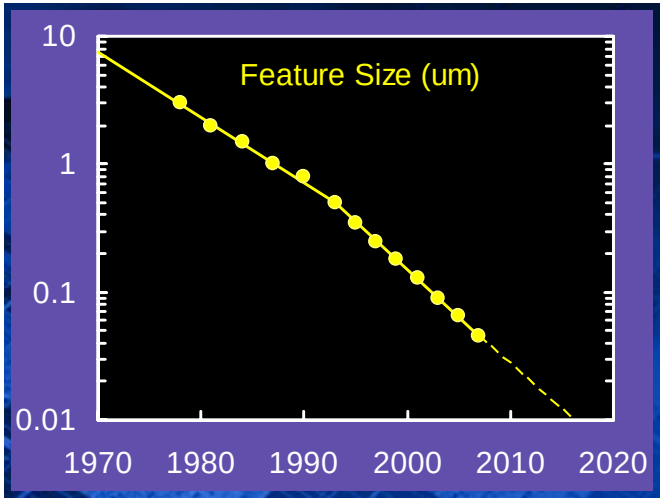
"The implementation of high-k and metal gate materials marks the biggest change in transistor technology since the introduction of polysilicon gate MOS transistors in the late 1960s"
Gordon Moore

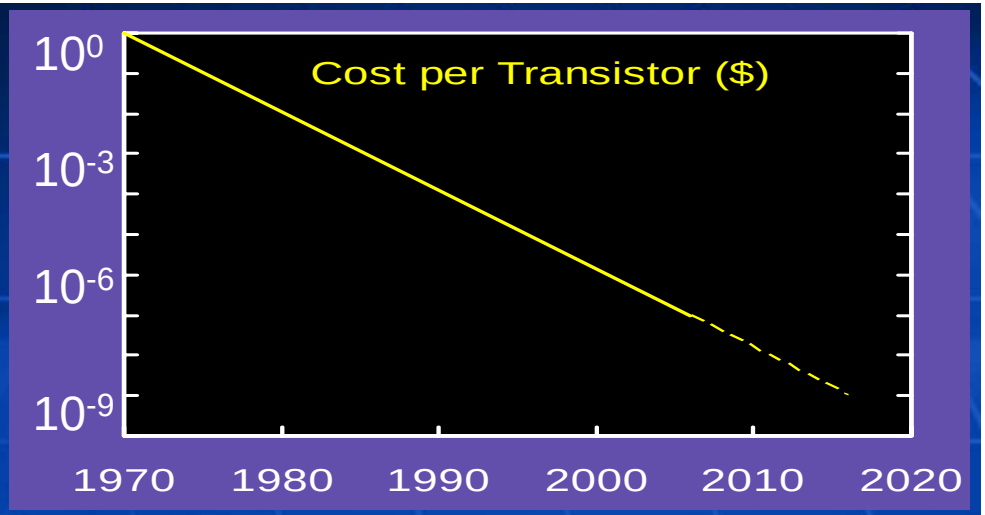
Intel's Logic Technology Evolution

Process Name:	P1262	P1264	P1266	P1268	P1270
Lithography:	90 nm	65 nm	45 nm	32 nm	22 nm
1st Production:	2003	2005	2007	2009	2011

Moore's Law continues!

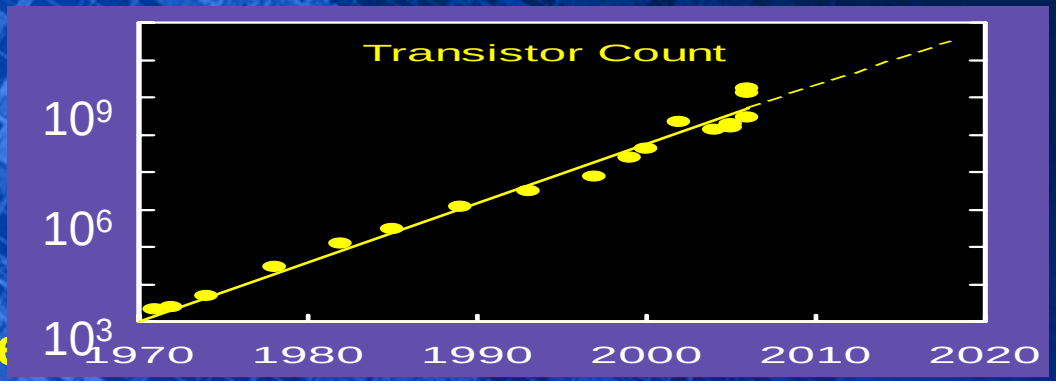
Intel continues to develop a new technology generation every 2 years





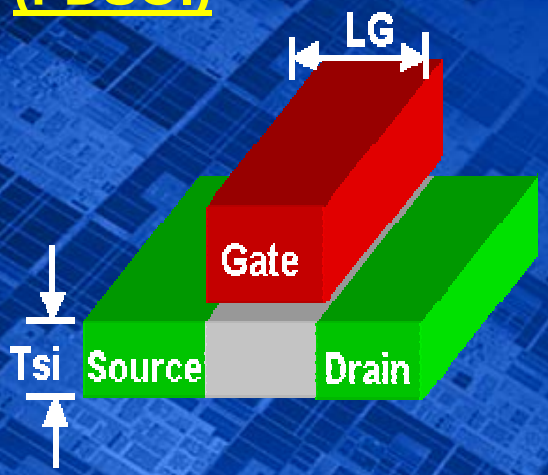
Moore's Law =

Transistor Budget +
Lowest Power and Lowest Cost



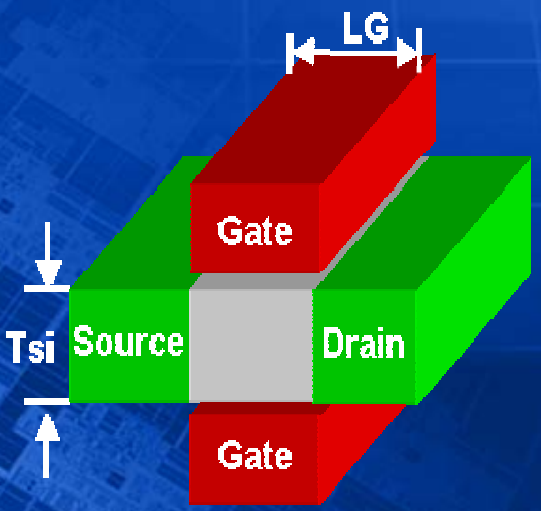
Fully Depleted Transistor Structures

Planar Single Gate (FDSOI)



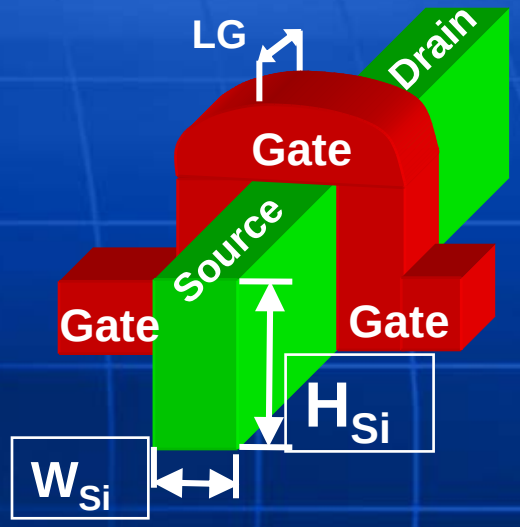
1. Ultra thin Tsi
2. Limited to SOI

Planar Double-Gate



1. Wider Tsi than planar
2. Non Self-aligned

Non Planar Tri-Gate



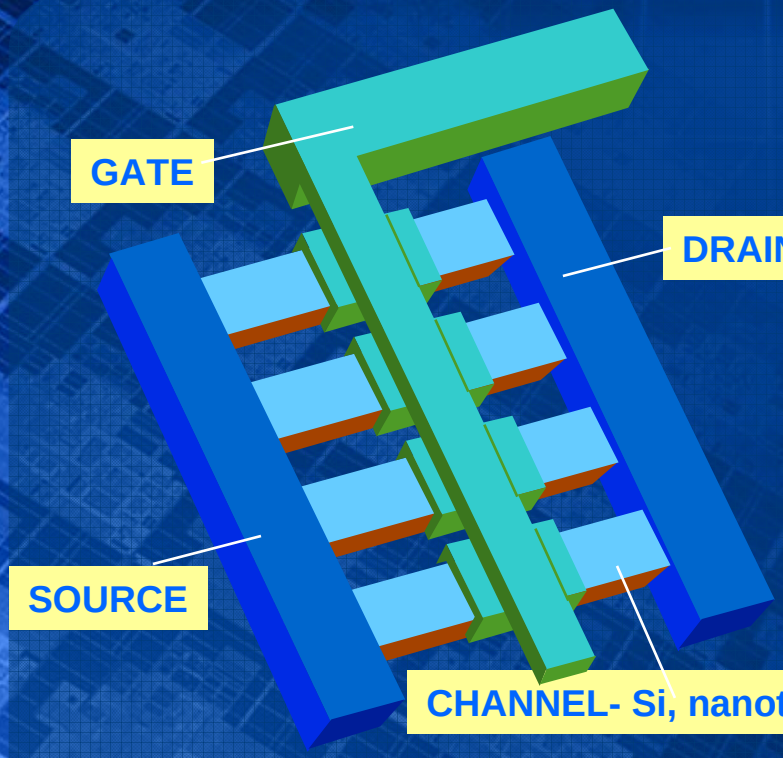
1. FIN W_{Si} is wider than planar T_{Si}
2. Self-Aligned gates
3. Bulk-Si or SOI

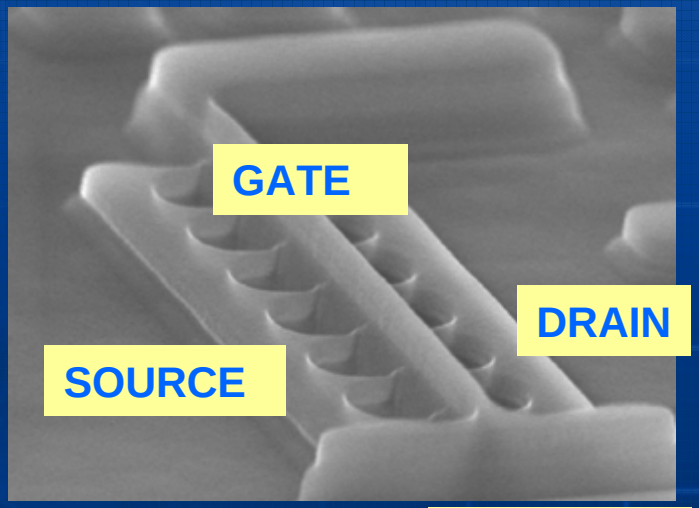
- Fully depleted thin-body devices improve SCE performance.
- Tri-Gate is the most favorable architecture for L_G scaling.

How Small is Small?

- ***Ultra Thin Body SOI (UTBSOI)***
  - Fully Depleted transistors have been demonstrated with Lg=25nm (Tsoi=6nm)
  - Simulations from University of California Berkeley show that UTBSOI can be scaled to Lg=12nm
  - Rule of thumb: Minimum Lg~2Tsoi
- ***Fin FET***
  - Good performance of FinFET demonstrated for sub-20nm Lg (W_{FIN}~10nm)
- Scalability of other ***multi-gate*** transistor structures reported

Tri-Gate Transistor:
"A template for the future"



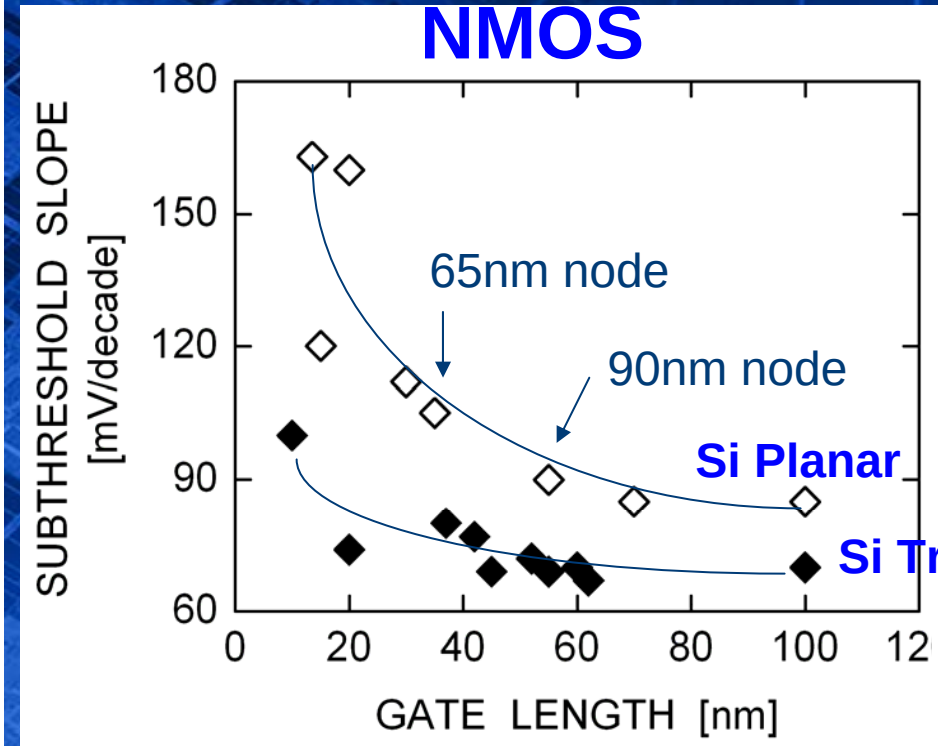


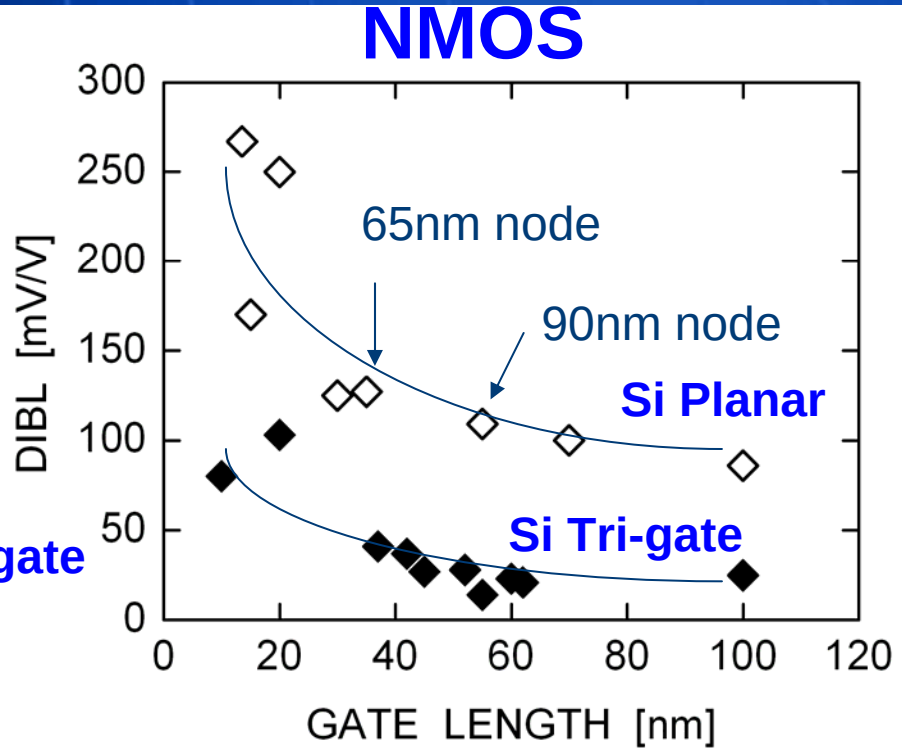
Source: Intel

CHANNEL- Si, nanotubes, nanowires …

Technical details presented at:
ISSDM Conference, Japan, Sept 17, 2002

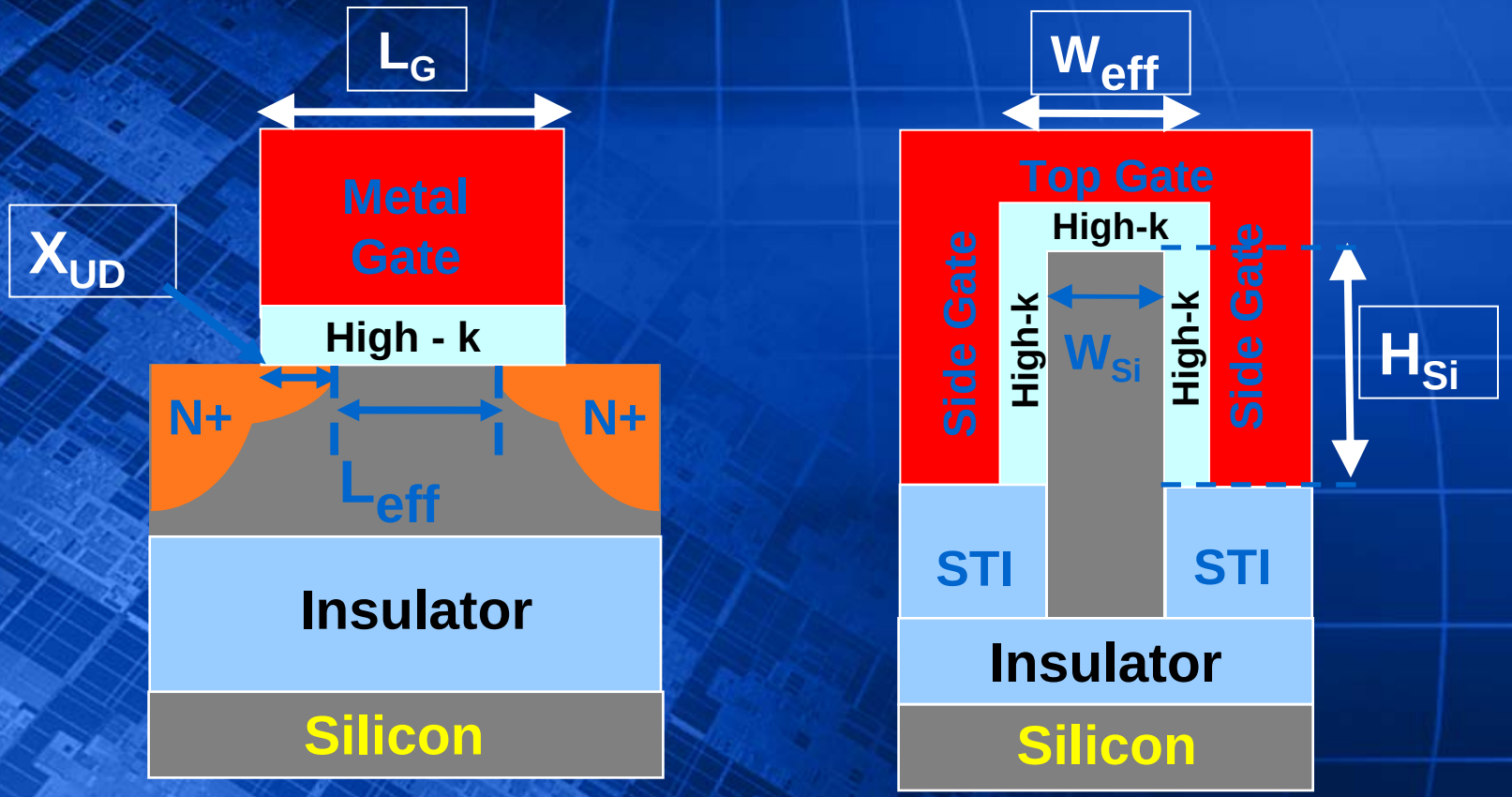
Benefits of Tri-Gate architecture





- Si planar transistors become exceedingly hard to scale
- Tri-gate architecture improves electrostatics significantly and extends transistor scalability

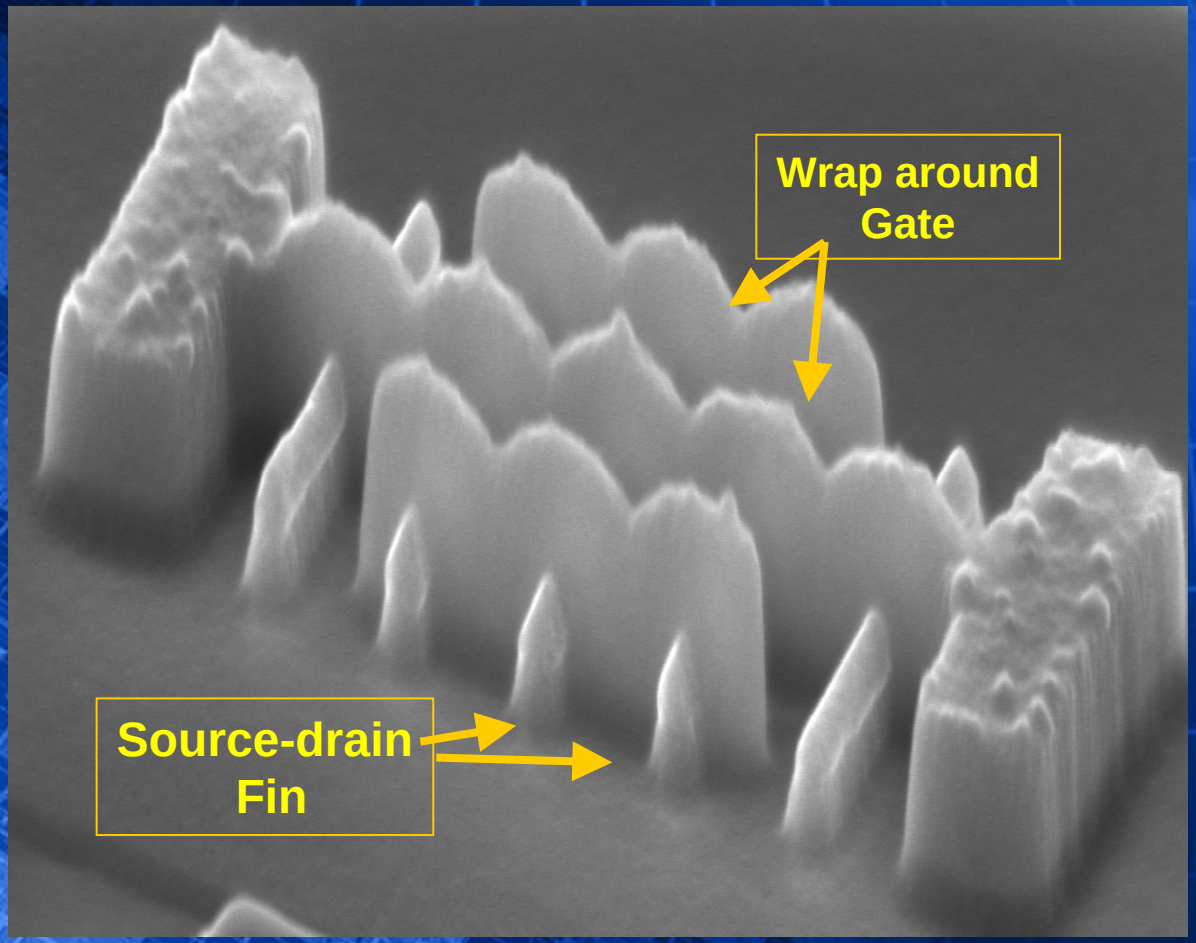
Tri-Gate Critical Dimensions



- I_{DSAT} is normalized by $Z_T = W_{Si} + 2*H_{Si}$
- Tri-gate electrostatics strongly depend on the ratio of L_{eff} / W_{eff} as defined by: $L_{eff} = L_G - 2 * X_{UD}$

$$W_{eff} = W_{Si} + 2(\varepsilon_{Si}/\varepsilon_{OX})*T_{OX}$$

The Key is Optimizing the Integration



1. Tri-gate gives better off current and therefore less wasted power
2. High k – metal gate gives both higher speed and less wasted power
3. Strained Si produces higher speed and less wasted power

The sum of all these pieces is once again world leading transistors

Picking the Right High-μ Material

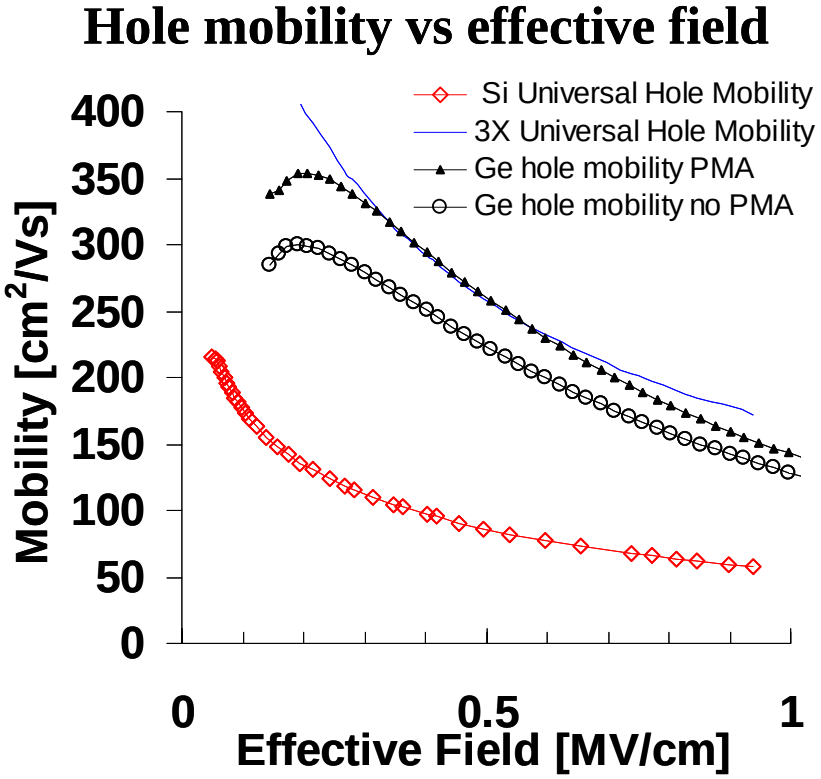
Material ⇒ Property ⇓	Si	Ge
Electron mobility	1600	3900
Hole mobility	430	1900
Bandgap (eV)	1.12	0.66
Dielectric constant	11.8	16

Why Ge?

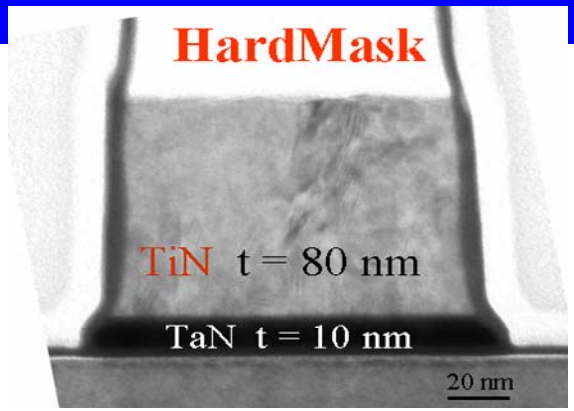
- **More symmetric and higher carrier mobilities**
  - **Highest hole mobility**
- **Easier integration on Si**
- **Lower temperature processing**

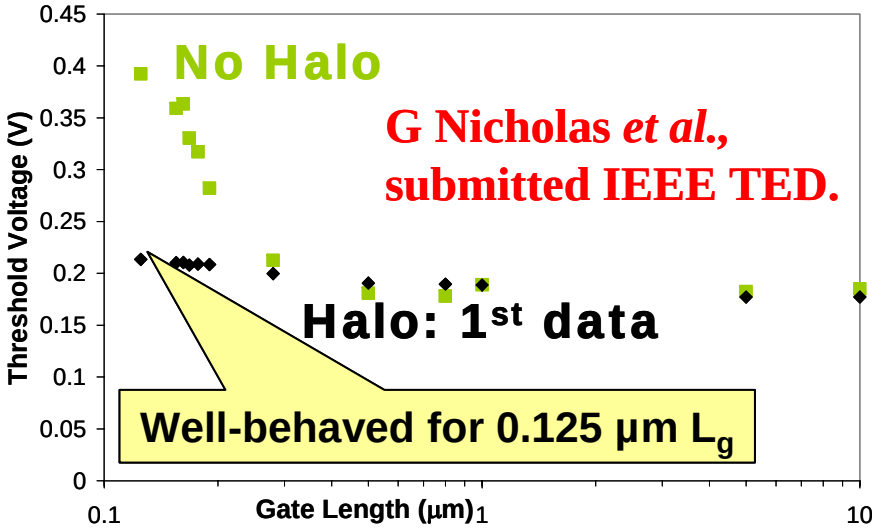
IMEC Ge pMOSFET

IMEC: M Meuris, M Heyns Intel: D Brunco, P Zimmerman



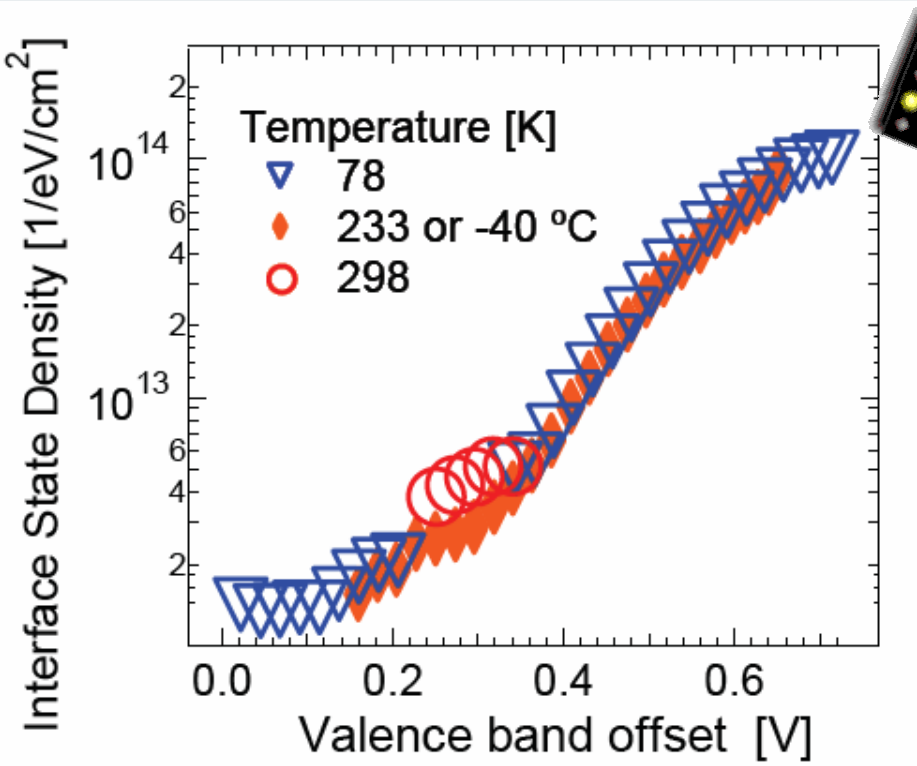
P Zimmerman *et al.*, IEDM 2006

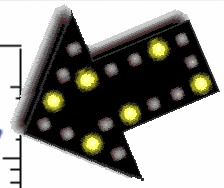




- Ge pMOS mobilities up to 358 cm²/Vs at 12 Å EOT with a gate leakage less than 0.01 A/cm² at V_t + 0.6 V. (6 ML of Epi-Si)
- High performance Ge pMOS transistors with L_g from 10 to 0.125 µm. (future target L_g to 50 nm)

Full conductance measurement at low temperature allows correct interface trap density extraction





IMEC's Si-passivated HfO_2 Ge MOSFETs

Acceptor type interface traps near the conduction band explain good performing pMOS

- traps are neutral and don't severely reduce channel mobility

and bad performing nMOS

- charged traps reduce mobility and lower amount of free carriers

imec

Increasing Electron Mobility

Increased mobility in the transistor channel leads to higher performance and less energy consumption

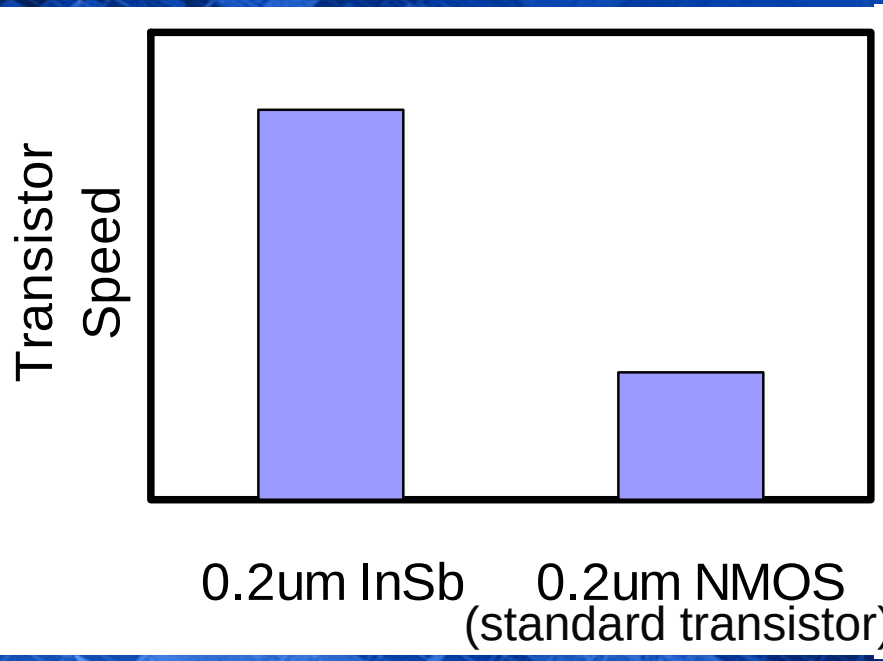
$$I_{DSAT} \propto \frac{W}{L} \cdot \mu \cdot C_{OX}$$

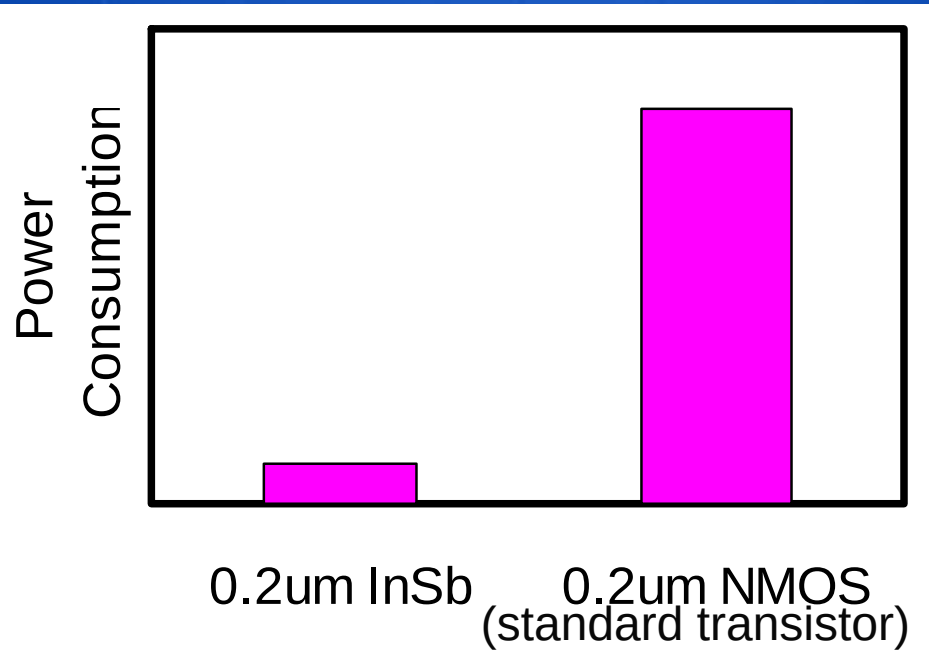
Relative mobility

	Compound Semiconductors		
Si	GaAs	InAs	InSb
1	8	33	50

Compound semiconductors have higher electron mobility than Si; InSb (indium antimonide) is highest of all

CMOS to continue for 15-20 years or more; Moore's Law could be extended indefinitely via new architectures, heterogeneous integration, 3D



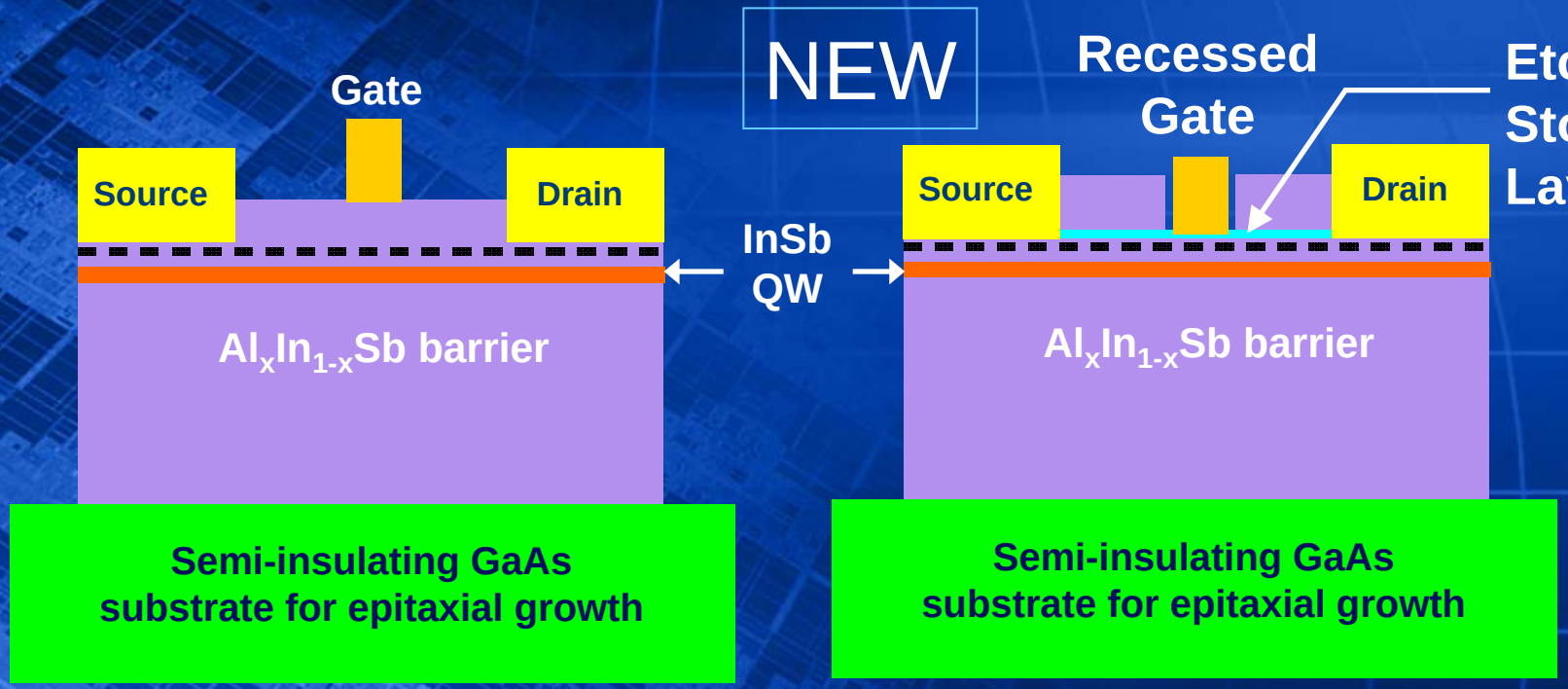


III/V is a 2015 Transistor option

- **3x faster or 10x lower power**
- **Integration with silicon key**

IEDM 2004

Depletion and Enhancement Mode

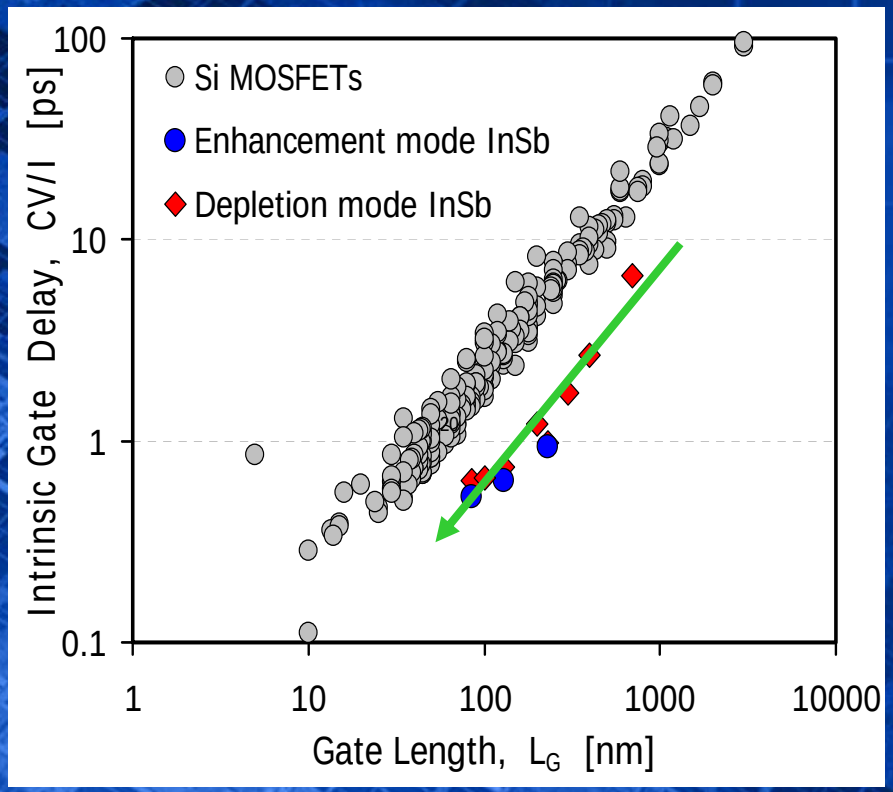


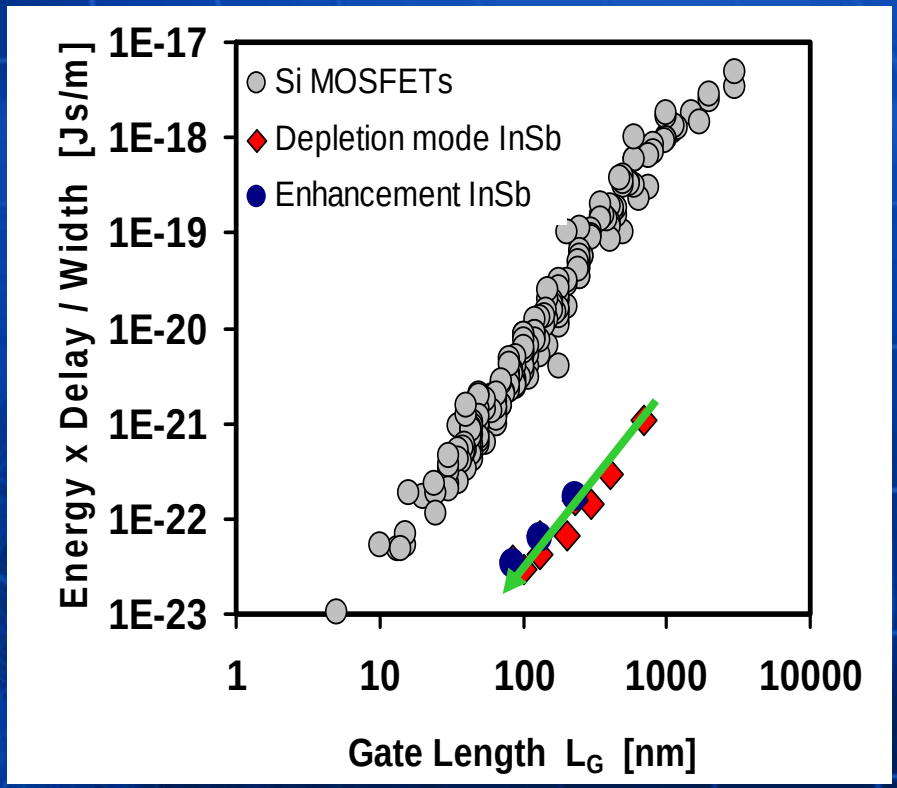
Depletion mode (Normally ON)

Enhancement mode (Normally OFF)

A novel gate recess process is used to fabricate enhancement mode InSb QWFETs

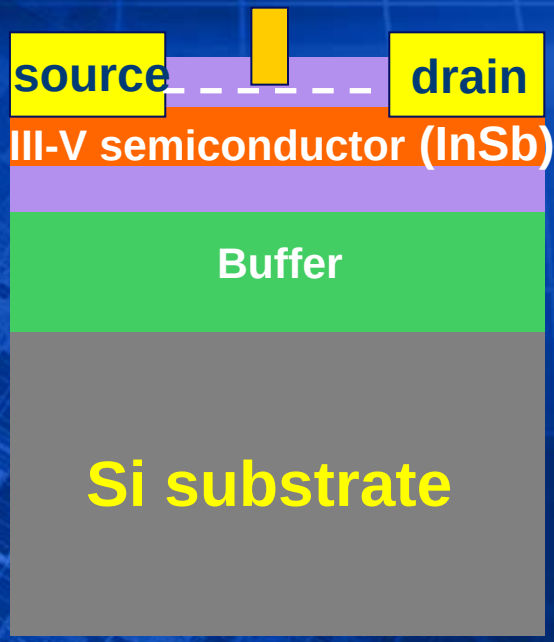
Benchmarking InSb QWFETs





InSb transistors show significant improvement in intrinsic gate delay and energy-delay product over Si MOSFETs at equivalent gate length

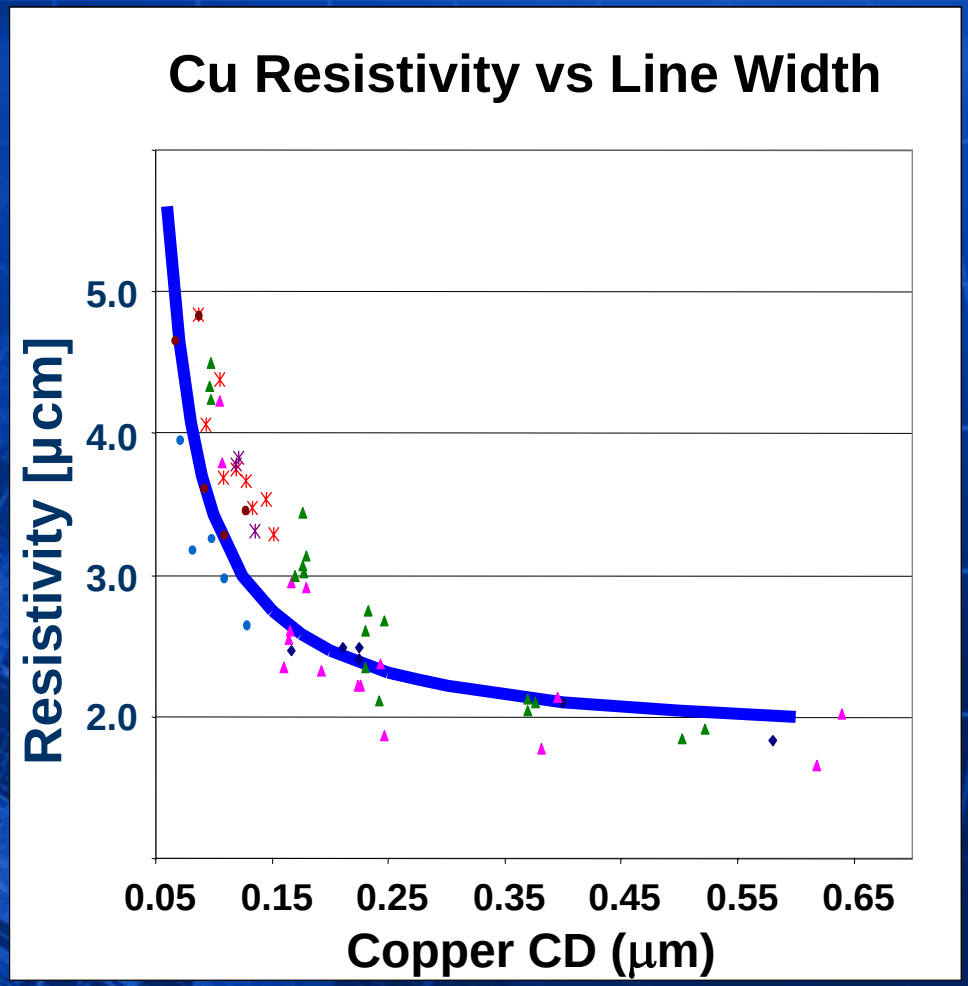
Integration on Si Platform



Current research on incorporation of new transistor onto the existing Si platform

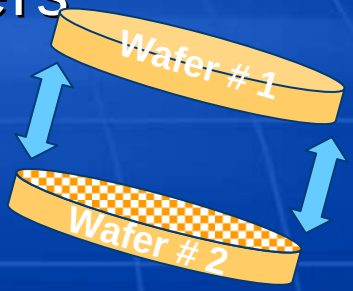
Metal Resistivity Scaling

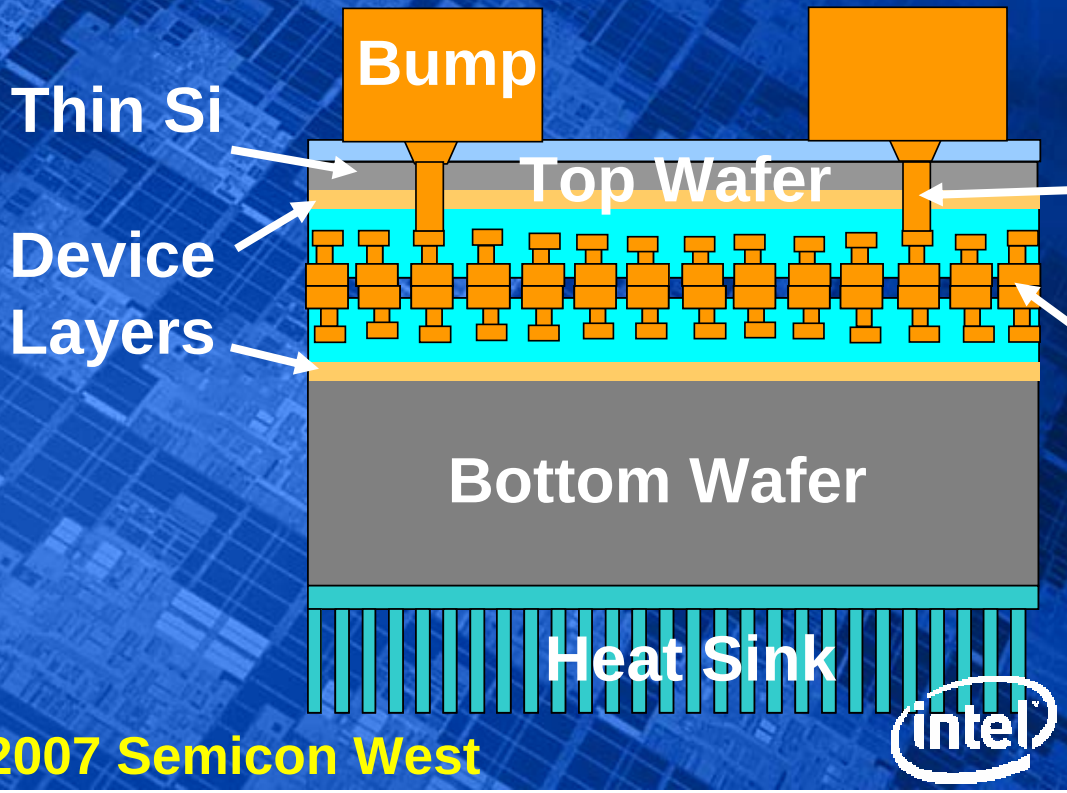
- Resistivity is a growing concern as line widths scale down
- Effect of liner thickness and electron scattering doubles effective resistivity as metal width scales from 150nm to 75nm
  - Feature size is approaching mean free path of electrons in Cu



3D Interconnects Research

- Cu bonding provides high-density low-resistance connections between device layers
- 300mm wafer-level stacking for fast throughput
- Through-Si Vias used for power and signal I/O

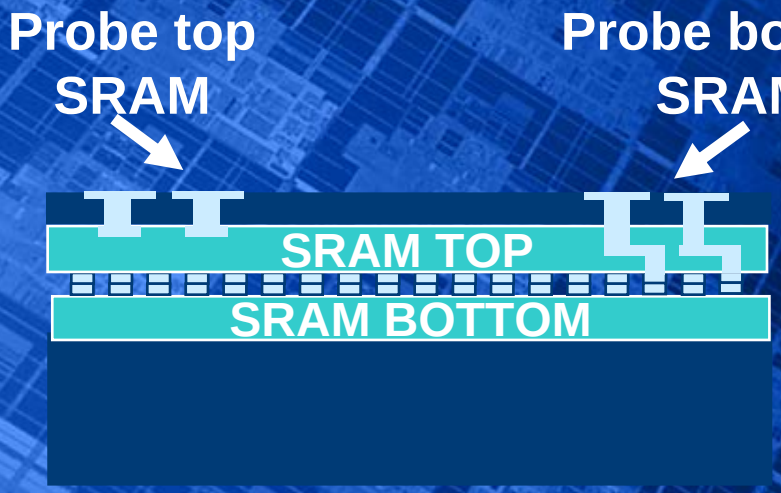


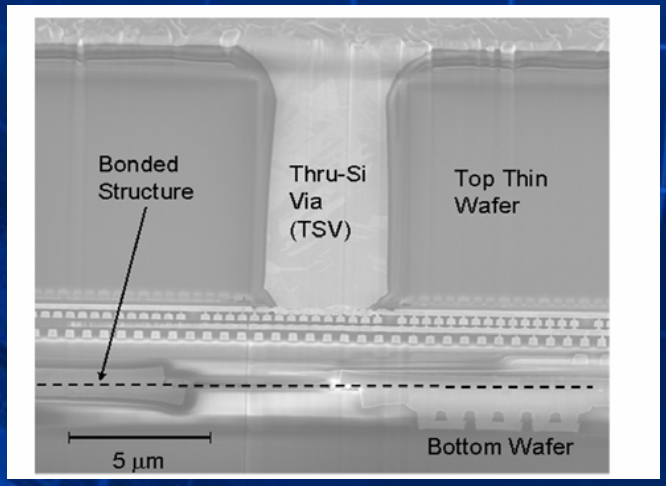


Bonding Layer (Cu)

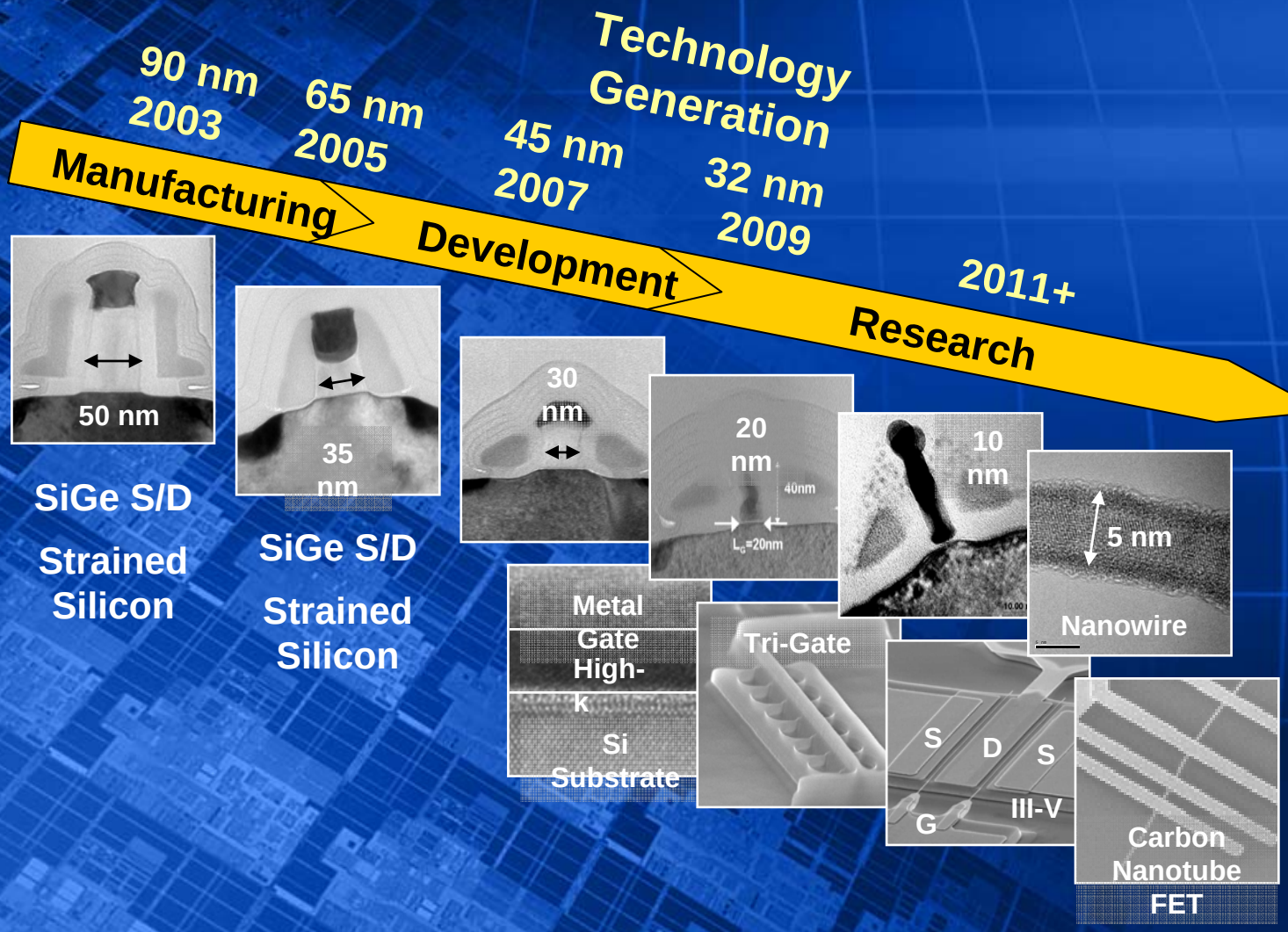
Stacked SRAMs

- SRAMs in both top (in thin silicon) and bottom silicon were functional
- SRAMs were probed using the through-Si Vias; the bottom SRAM is probed through the bonding layer





Transistor Nanotechnology



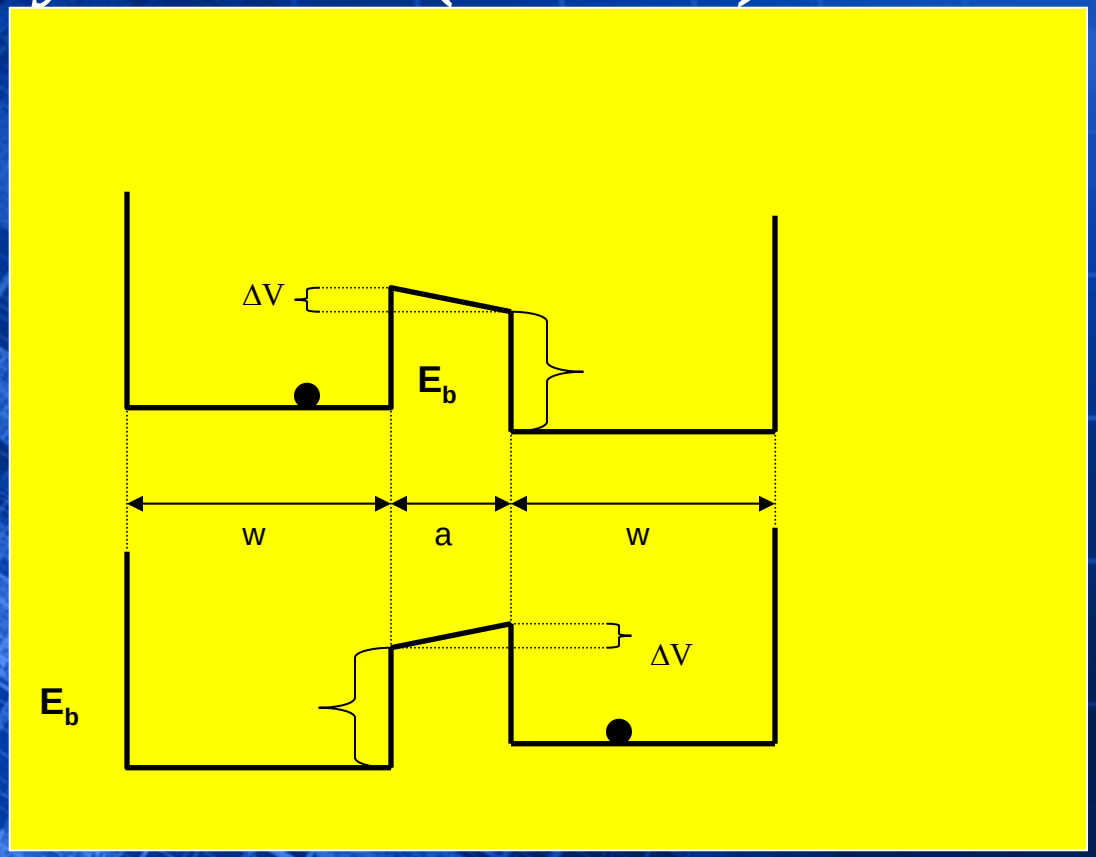
External research ~2020

Spin
Molecular
Optical
Phase
Other
?????

Source: Intel

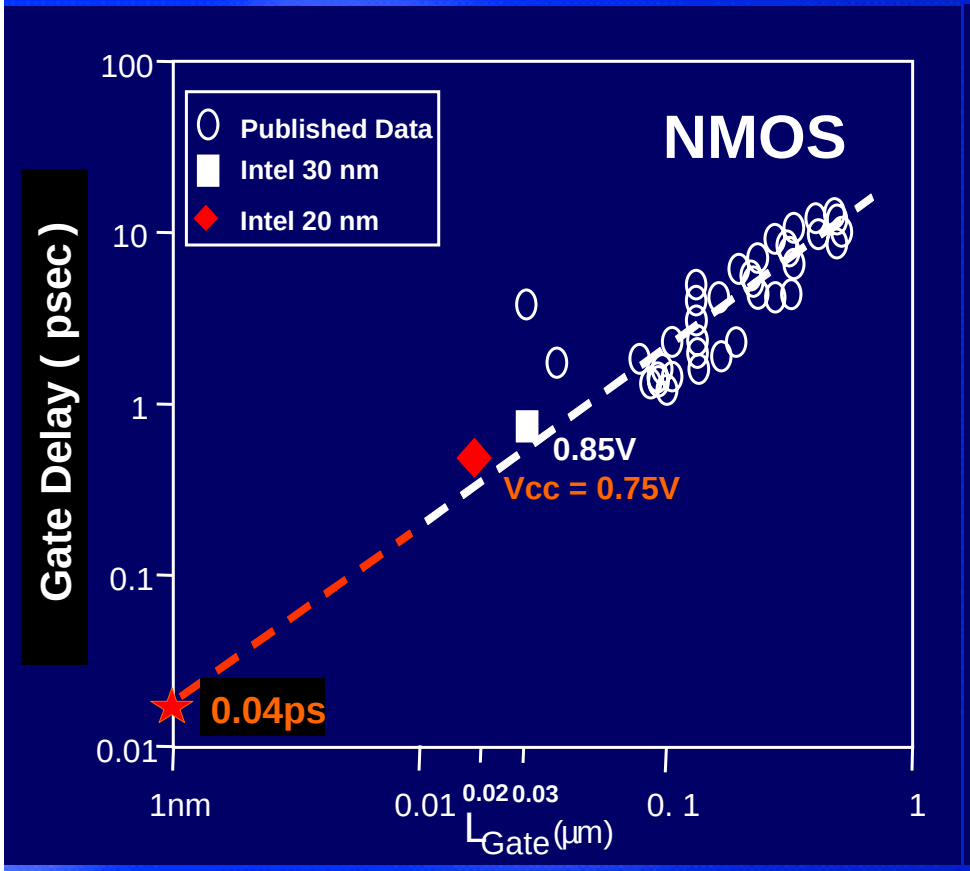
Future options subject to change

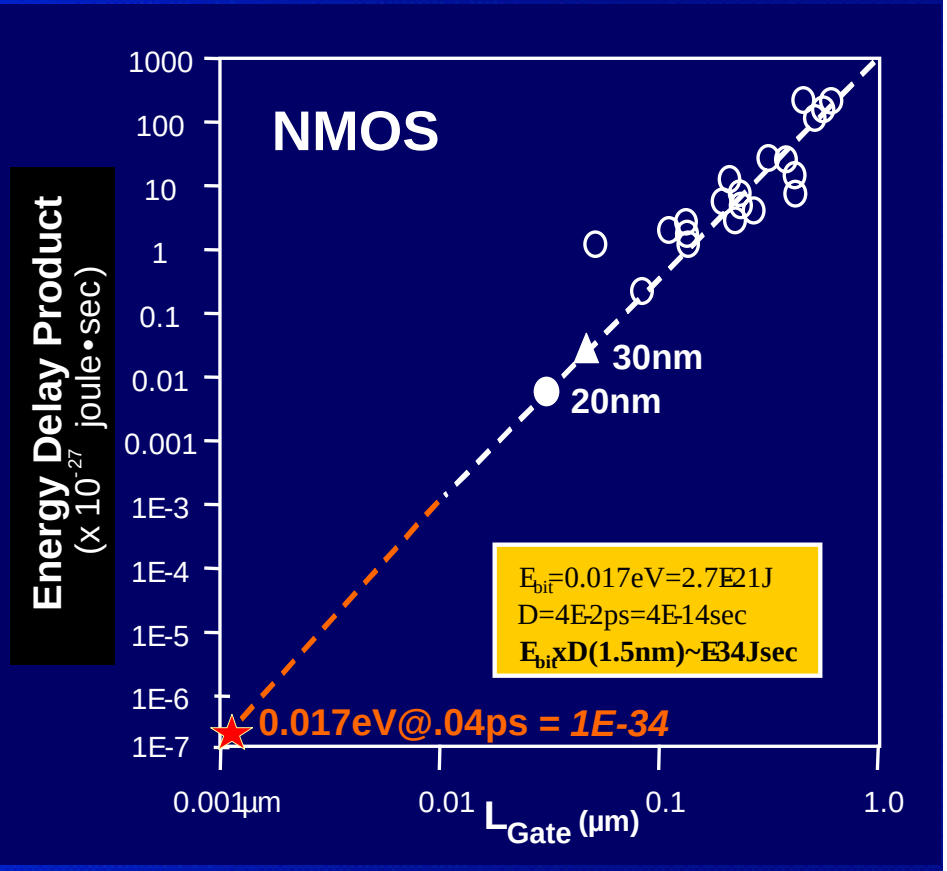
The field effect transistor (FET) can be thought of as consisting of two wells (source and drain) separated by a barrier (channel).



w = width of Left-Hand Well (LHW) and Right-Hand Well (RHW)
a = barrier width
E_b = barrier energy,

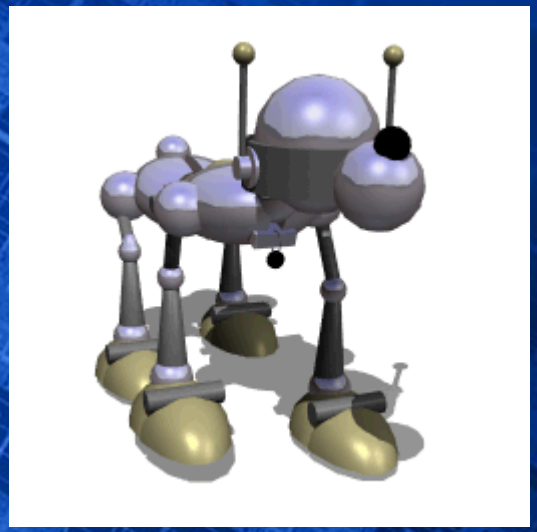
Theoretical to Experimental



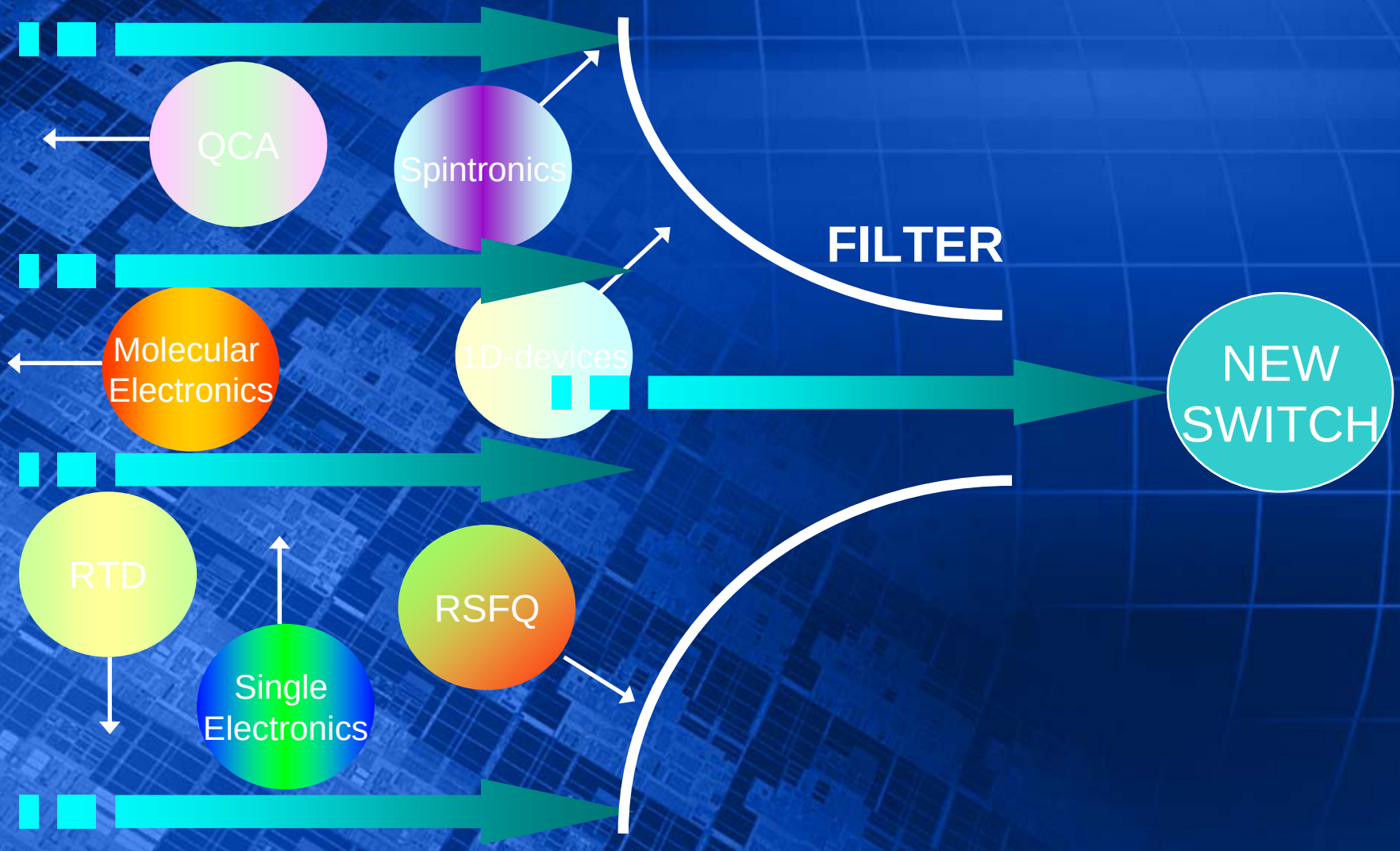


Current MOS device operation scales close to ideal

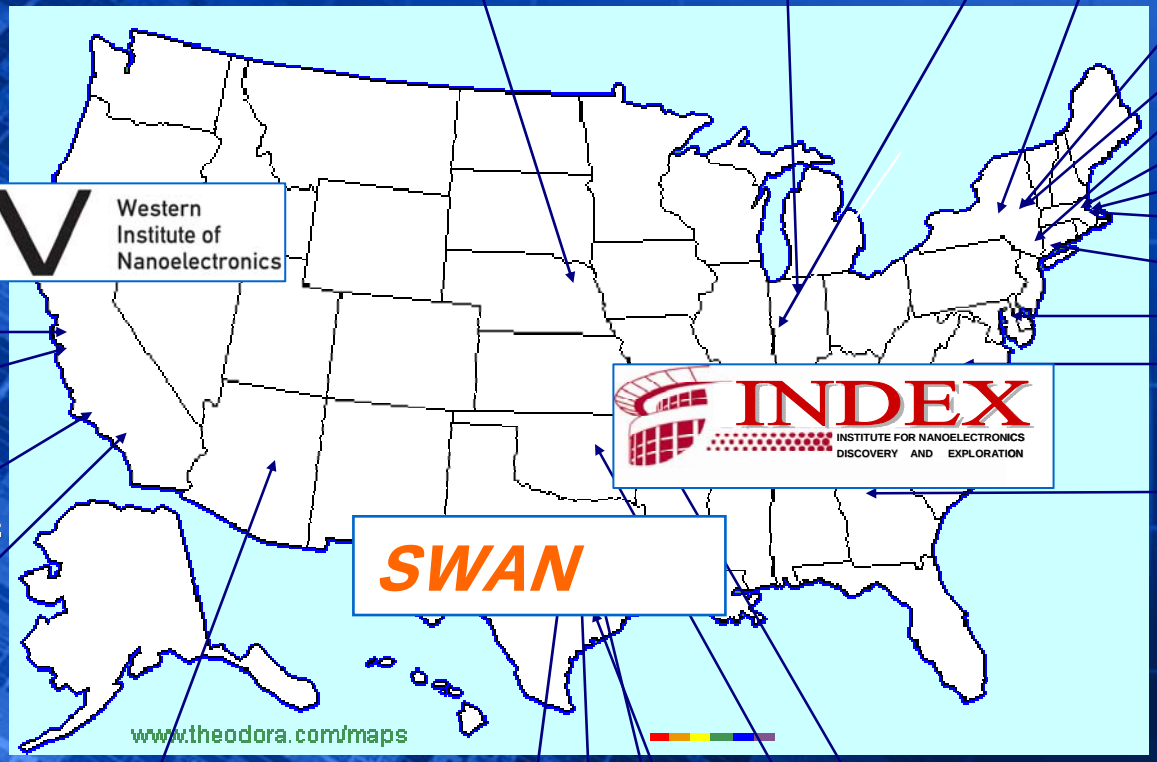
Beyond CMOS



Which current Nanoelectronic concept will become the NEW SWITCH?



NRI Funded Universities



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Notre Dame

Cornell

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RPI

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U Mass

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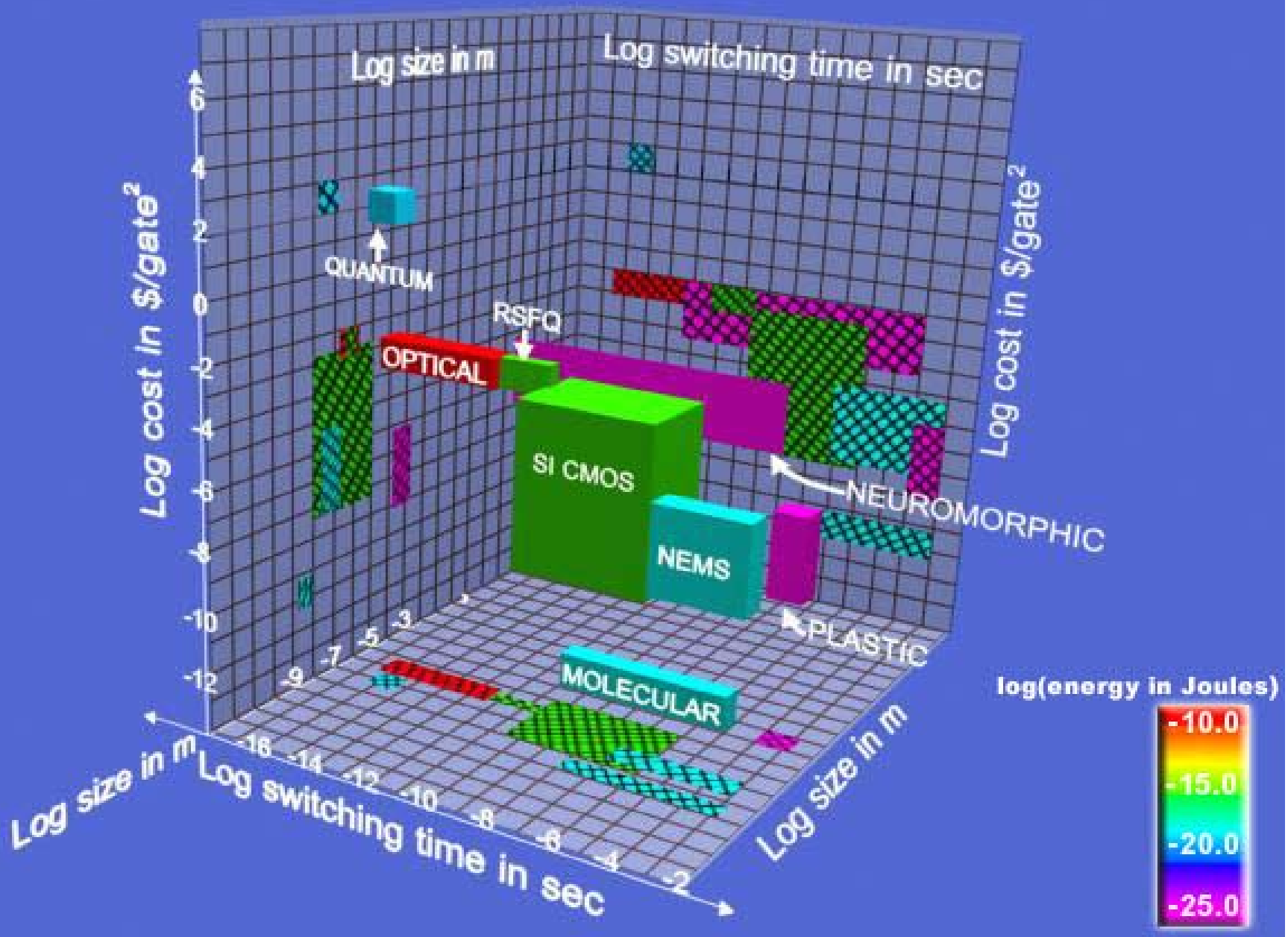
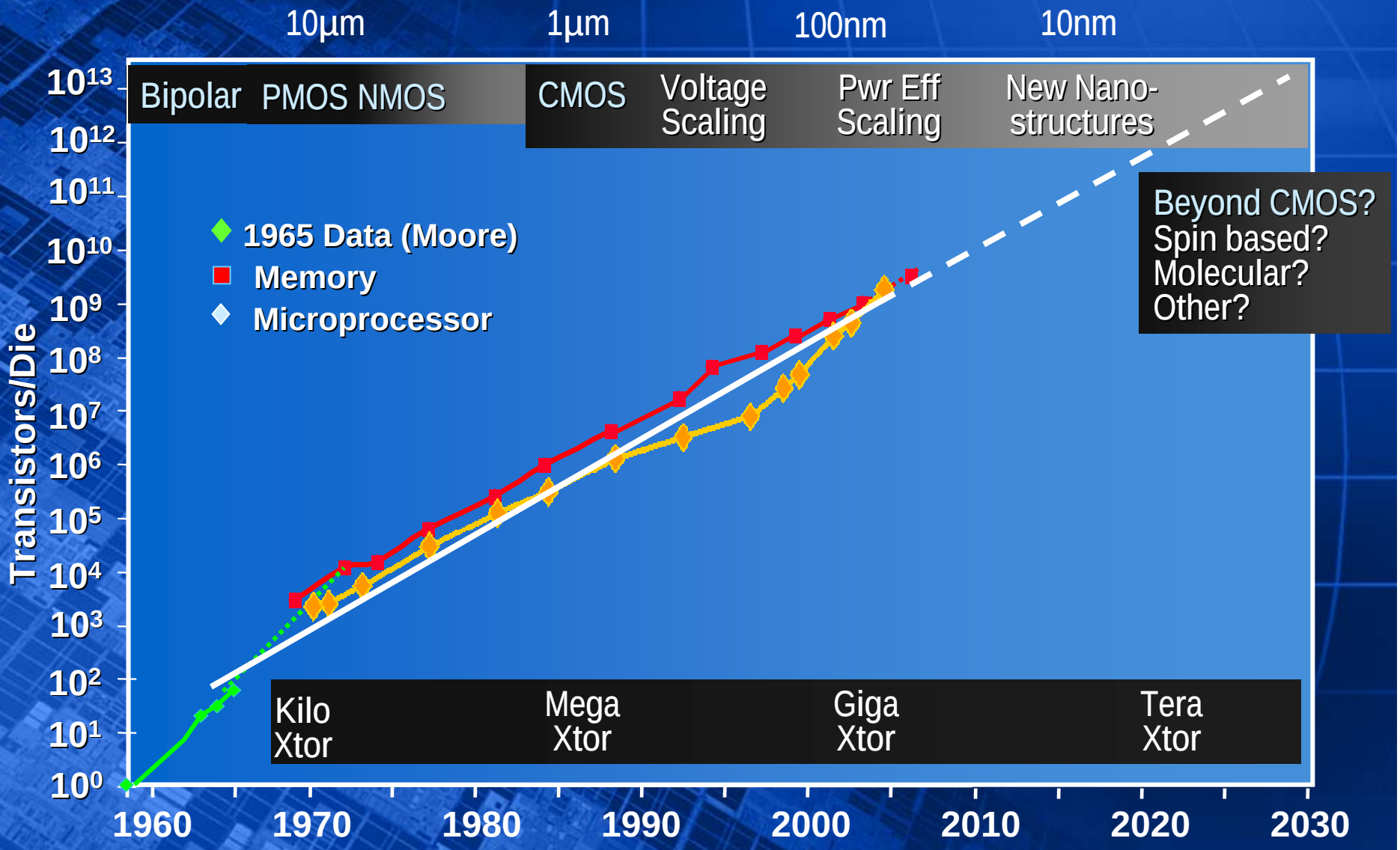
Emerging Technology Parametrization



Looking ahead

Moore's Law Will Outlive CMOS



Thank you for your attention